Ramon Canal

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KEY FIGURES

Publications total (peer reviewed)	106	Industry / Academic Seminars	7
Total citations	>2000	Invited talks/keynotes/panels	13
H-index	22	Personal Awards	7
G-index	43	Publication Awards	7
Scientific Committees (Program Committees)	47	Projects (PI)	5
Commissions of trust (Editorial/Project evaluation board, Conference Organization, International PhD Assessment board)	15	Projects (WP leader/Key personnel)	10
Institutional positions (Vice-dean, deputy head)	3	Projects (total)	19

EDUCATION

2004 PhD in Computer Architecture– Universitat Politècnica de Catalunya (UPC), Spain Advisors: James E. Smith (U. of Wisconsin-Madison, USA), Antonio González (UPC)

1998 Engineering degree in Computer Science (equivalent MSc+BSc). Universitat Politècnica de Catalunya, Spain Final year done at the University of Bath, UK.

POSITIONS

2023 – Professor, Barcelona School of Informatics, UPC, Spain
2018 – Part-time research associate, Barcelona Supercomputing Center, BSC, Spain
2008 – 2023 Associate Professor, Barcelona School of Informatics, UPC, Spain
2003 – 2008 Assistant Professor, Barcelona School of Informatics, UPC, Spain

PREVIOUS POSITIONS (MOBILITY)

2019 – 2020 Visiting Professor, University of Cyprus, Nicosia, Cyprus.
2006 – 2007 Visiting Scholar, Harvard University, Cambridge (Massachusetts), USA.
2003 – 2006 Lecturer, School of Engineering, Universitat Ramon Llull (URL), Spain
2000/6–2000/10 Researcher, Sun Microsystems, Sunnyvale (California), USA.

INSTITUTIONAL RESPONSIBILITIES

2013 – 2017 Vice dean of Postgraduate Studies, Barcelona School of Informatics, UPC, Spain.
2010 – 2013 Coordinator of the Undergraduate Computer Engineering Curricula, Barcelona School of Informatics, UPC, Spain
2008 – 2011 Deputy Head of the Department of Computer Architecture, UPC, Spain

AWARDS

2016 Senior member elevation, IEEE Computer Society.
2006-2007: Fulbright Award. Visiting Scholar, Harvard University (Fulbright association). (40,000€)
'10,'13, '18: Excellence in Education Award. UPC and AQU-University Quality Control Agency.
2008: First prize, 6th Duran Farell Award in Innovation and Technology in Spain. (60,000€)
2001: First prize, "Rosina Ribalta" awards of the Epson Foundation Spain and Portugal. (12,000€)
2000: IBM Faculty Award for my work in value compression. (80,000$)
7 Paper Awards: ICCD ('14), DCIS ('12), HiPEAC Paper Award ('09. '10, '13, '17), HPCA ('00)

SUPERVISION OF GRADUATE STUDENTS AND POSTDOCTORAL FELLOWS

Current: 1 PostDoc, 2 research staff, 1 MSc and 1 BSc
Past: 1 PostDoc, 4 PhD, 21 MSc and 10 BSc students

CURRENT TEACHING ACTIVITIES (UPC, Spain)

Master level – (1) Nanotechnology Circuit Design and (2) Processor Design
Undergrad level – (3) Computer Architecture and (4) VLSI

COMMISSIONS OF TRUST / EVALUATION BOARD

2020 Expert Reviewer for Italian Scientific Evaluation, Italian Ministry of University and Research.
2009, 2010 Scientific Advisory Board, Fulbright Award selection committee in Spain.
2009 Evaluator, Nederlandse Organisatie voor Wetenschappelijk Onderzoek - Netherlands Organisation for Scientific Research (NWO).

COMMISSIONS OF TRUST / ORGANISATION OF SCIENTIFIC MEETINGS and EDITOR of JOURNALS

2019 – Associate Editor Transactions on Architecture and Code Optimization, ACM.
2016 – Associate Editor Journal of Parallel and Distributed Computing, Elsevier.
2022 Industrial co-chair. IEEE ETS, Barcelona (Spain)
2019 Program track co-chair. IEEE DATE, Florence (Italy)
2016 General co-chair. IEEE/ACM HPCA, Barcelona (Spain)
2014 Students chair, IEEE/ACM CGO, Orlando (Florida, USA)
2012 General co-chair 18th IEEE IOLTS, Sitges (Spain).

COMMISSIONS OF TRUST / SCIENTIFIC COMMITTEES

Program committee member (selection of 11 highest ranked conferences)
‘11, ’13, ’17 - ‘23 IEEE/ACM International Symposium on Computer Architecture (ISCA)
’12-’14, ’18 - ’23 IEEE/ACM Int. Symposium on High Performance Computer Architecture (HPCA)
’17, ’20 - ‘22 IEEE/ACM International Symposium on Microarchitecture (MICRO)
‘08, ’10, ’16 -‘22 IEEE International Conference on High Performance Computing (HiPC)
’17, ’18,’19 IEEE Design, Automation and Test in Europe Conference (DATE)
‘06, ’08, ‘17 IEEE International Conf. on Computer Design (ICCD)
’16 IEEE Micro Top Picks
‘14, ‘16 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)
’13, ‘14 IEEE/ACM Conference on Supercomputing (SC)
‘09, ’14, ‘19 IEEE/ACM International Parallel and Distributed Processing Symposium (IPDPS)
Board of Reviewers
2004 – Regularly in IEEE and ACM conferences and journals such as: ISCA, MICRO, HPCA, ASPLOS, PACT, ICS, EUROPAR, CGO, IPDPS, ICPADS, ICCD, ISCAS, HiPEAC, IEEE Micro, IEEE Micro Top Picks, IEEE Transactions on Computers, IEEE Transaction on VLSI Systems, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Evolutionary Computing, IET Circuits, Devices & Systems, ACM Transactions on Architecture and Code Optimization, Journal of Systems Architecture.

COMMISSIONS OF TRUST / ACADEMIC COMMITTEES (International PhD Evaluation Panels)

Chalmers University of Technology (Goteborg, Sweden), 2016, 2017 and 2021.
Politecnico di Torino (Torino, Italy), 2017, 2021
CNRS Montpellier (Montpellier, France), 2016

MEMBERSHIPS OF SCIENTIFIC SOCIETIES

2016 – Senior member of the IEEE Computer Society, Worldwide (previously member).
2004 – Member, Research Network of Excellence (UE) “HiPEAC”, EU
2002 – Member of the ACM and ACM SIGARCH interest group. Worldwide.
2000 – Funding member of the Spanish Society of Computer Architecture and Technology (SARTECO), Spain
1999 – Member of the Official College of Computer Science Engineers of Catalonia (COEIC), Catalonia, Spain

RESEARCH PROJECTS

EU Funding

2023-2025	PI/ Coordinator	Vitamin-V: Virtual Environment and Tool-boxing for Trustworthy Development of RISC-V based Cloud Services. Horizon Europe (HE-101093062)
2022-2025	Key personnel	EUMaster4HPC: Hpc EuRopean ConsortiUm Leading Education activities (H2020-101051997)
2021-2023	WP Leader	FRACTAL: Cognitive Fractal and Secure Edge Based On Unique Open-Safe-Reliable-Low Power Hardware Platform Node (ECSEL-877056)
2018-2021	WP Leader	RECIPE: REliable power and time-ConstraInts-aware Predictive management of heterogeneous Exascale systems (H2020-801137)
2019-2020	PI	Fast virtual SoC for advanced GPS algorithm evaluation (H2020-800962). EuroLab4HPC2 subproject.
2013-2016	WP Leader	CLERECO: Cross-layer early reliability evaluation for the computing continuum (FP7-611404)
2010-2012	Key personnel	TRAMS: Terascale Reliable Adaptive Memory Systems (FP7-248789)
1997-2000	Member	MHAOTEU: Memory Hierarchy Analysis and Optimisation Tools for the End-User (ESPRIT PROJECT 24942)

National Funding

2019-2022	Local PI	DRAC: Disseny d'acceleradors basats en la tecnologia RISC per a la propera generació de computadors (RIS3CAT IU16-011643)
2019-2022	PI	Resiliencia Unificada para Sistemas Informáticos (EIN2019-102930)
2019-2022	Key personnel	Mejora de la infraestructura científico-técnica del Departamento de Arquitectura de Computadores de la UPC (EQC2019-005653-P)
2019-2022	Key personnel	Investigación, formación y prospectiva en sistemas RISC-V (RED2018-102384-T)
2017-2019	PI	Encapsulado de herramientas virtual para una gestión robusta de la heterogeneidad entre capas en sistemas ciberfísicos complejos (EUIN2017-85841)
2014-2017	WP Leader	Microarquitectura y Compiladores para Futuros Procesadores III (TIN2013-44375-R)
2011-2014	WP Leader	Microarquitectura y Compiladores para Futuros Procesadores II (TIN2010-18368)
2008-2010	WP Leader	Microarquitectura y Compiladores para Futuros Procesadores (TIN2007-61763)
2004-2007	Member	Computación de Altas Prestaciones IV: arquitecturas, compiladores, sistemas operativos, herramientas y aplicaciones (TIN2004-07739-C02-01)
2001-2004	Member	Computación de Altas Prestaciones III: Arquitecturas, Compiladores, Sistemas Operativos, Herramientas y Algoritmos (TIC2001-0995-C02-01)
1998-2001	Member	Computación de Altas Prestaciones II: Arquitecturas, Compiladores, Sistemas Operativos, Herramientas y Aplicaciones (TIC98-0511-C02-01)

PUBLICATIONS (Highest 30th cited papers)

Cites	Authors	Title	Year	Venue
169	R Canal, A González, JE Smith	Very low power pipelines using significance compression	2000	MICRO
166	R Canal, JM Parcerisa, A González	Dynamic cluster assignment mechanisms	2000	HPCA
137	X Liang, R Canal, GY Wei, D Brooks	Process variation tolerant 3T1D-based cache architectures	2007	MICRO
132	R Canal, A González	A low-complexity issue logic	2000	ICS
124	M Monchiero, R Canal, A González	Design space exploration for multicore architectures: a power/performance/thermal view	2006	ICS
88	M Monchiero, R Canal, A Gonzalez	Power/performance/thermal design-space exploration for multicore architectures	2008	IEEE Trans. On Parallel and Distributed Systems
88	R Canal, A González	Reducing the complexity of the issue logic	2001	ICS
86	R Canal, JM Parcerisa, A Gonzalez	A cost-effective clustered architecture	1999	PACT
82	E Herrero, J González, R Canal	Elastic cooperative caching: an autonomous dynamically adaptive memory hierarchy for chip multiprocessors	2010	ISCA
81	N Jing, Y Shen, Y Lu, S Ganapathy, Z Mao, M Guo, R Canal, X Liang	An energy-efficient and scalable eDRAM-based register file architecture for GPGPU	2013	ISCA
68	E Herrero, J González, R Canal	Distributed cooperative caching	2008	PACT
53	X Liang, R Canal, GY Wei, D Brooks	Replacing 6T SRAMs with 3T1D DRAMs in the L1 data cache to combat process variability	2008	IEEE micro
47	M Kaliorakis, D Gizopoulos, R Canal, A Gonzalez	Merlin: Exploiting dynamic instruction behavior for fast and accurate microarchitecture level reliability assessment	2017	ISCA
46	A Valero, J Sahuquillo, S Petit, V Lorente, R Canal, P López, J Duato	An hybrid eDRAM/SRAM macrocell to implement first-level data caches	2009	MICRO
46	J Abella, R Canal, A González	Power-and complexity-aware issue queue designs	2003	IEEE micro
36	S Ganapathy, R Canal, A Gonzalez, A Rubio	Circuit propagation delay estimation through multivariate regression-based modeling under spatio-temporal variability	2010	DATE
31	R Canal, JM Parcerisa, A González	Dynamic code partitioning for clustered architectures	2001	Int. J. of Parallel Programming
29	A Vallero, et al.	Cross-layer system reliability assessment framework for hardware faults	2016	ITC
29	M Riera, R Canal, J Abella, A Gonzalez	A detailed methodology to compute soft error rates in advanced technologies	2016	DATE
28	R Canal, A González, JE Smith	Software-controlled operand-gating	2004	CGO

25	A Vallero, et al.	Syra: Early system reliability analysis for cross-layer soft errors resilience in memory arrays of microprocessor systems	2018	IEEE Trans. on Computers
23	M Anglada, R Canal, JL Aragón, A González	MASkIt: Soft error rate estimation for combinational circuits	2016	ICCD
22	E Herrero, J Gonzalez, R Canal	Distributed cooperative caching: An energy efficient memory scheme for chip multiprocessors	2011	IEEE Trans. on Parallel and Distributed Systems
19	E Herrero, J Gonzalez, R Canal, D Tullsen	Thread row buffers: Improving memory performance isolation and throughput in multiprogrammed environments	2012	IEEE Trans. on Computers
18	N Aymerich, S Ganapathy, A Rubio, R Canal, A Gonzalez	Impact of positive bias temperature instability (PBTI) on 3T1D-DRAM cells	2011	GLSVLSI
17	Z Jakšić, R Canal	Enhancing 6T SRAM cell stability by back gate biasing techniques for10nm SOI FinFETs under process and environmental variations	2012	MIXDES
17	A Rubio, J Figueras, EI Vatajelu, R Canal	Process variability in sub-16nm bulk CMOS technology	2012	upccommons
15	Z Jaksic, R Canal	Comparison of SRAM cells for 10-nm SOI FinFETs under process and environmental variations	2012	IEEE Trans. on electron devices
14	E Amat, A Calomarde, F Moll, R Canal, A Rubio	Feasibility of embedded DRAM cells on FinFET technology	2014	IEEE Trans. on Computers
14	S Ganapathy, R Canal, et al.	A novel variation-tolerant 4T-DRAM cell with enhanced soft-error tolerance	2012	ICCD

PUBLICATIONS (2017-2022)

Cites	Authors	Title	Year	Source
0	SM León, BO Calviño, LA Vivas, RC Corretger, OR Ulacio	Small-layered Feed-Forward and Convolutional neural networks for efficient P wave earthquake detection	2022	Expert Systems with Applications
0	E Rodríguez, P Valls, B Otero, JJ Costa, J Verdú, MA Pajuelo, R Canal	Transfer-Learning-Based Intrusion Detection Framework in IoT Networks	2022	Sensors
0	Y Sazeides, A Bramnik, R Gabor, R Canal	A Real-Time Error Detection (RTD) Architecture and its use for Reliability and Post-Silicon Validation for F/F based Memory Arrays	2022	IEEE Trans. on Emerging Topics in Computing
0	R Canal, F Bas, S Alcaide, G Cabo, P Benedicte, F Fuentes, et al.	SafeDX: Standalone Modules Providing Diverse Redundancy for Safety-Critical Applications	2022	SAMOS
10	E Rodriguez, B Otero, N Gutierrez, R Canal	A survey of deep learning techniques for cybersecurity in mobile networks	2021	IEEE Communications Surveys &Tutorials
1	B Otero, E Rodríguez, O Rojas, J Verdú, JJ Costa, et al.	A cost-efficient QoS-aware analytical model of future software content delivery networks	2021	International Journal of Network Management
1	R Canal, Y Sazeides, A Bramnik	SRAM arrays with built-in parity computation for real-time error detection in cache tag arrays	2021	DATE
0	N Gutiérrez, B Otero, E Rodríguez, R Canal	Malicious Website Detection Through Deep Learning Algorithms	2021	LOD
0	A Lasheras, R Canal, E Rodríguez, L Cassano	Securing RSA hardware accelerators through residue checking	2021	Microelectronics Reliability
12	G Agosta, W Fornaciari, D Atienza, R Canal, A Cilardo, et al.	The RECIPE approach to challenges in deeply heterogeneous high performance systems	2020	Microprocessors and Microsystems
8	R Canal, C Hernandez, R Tornero, A Cilardo, et al.	Predictive reliability and fault management in exascale systems: State of the art and perspectives	2020	ACM Computing Surveys (CSUR)
6	P Radojkovic, M Marazakis, P Carpenter, et al.	Towards resilient EU HPC systems: A blueprint	2020	European HPC resilience initiative
5	Y Sazeides, A Bramnik, R Gabor, C Nicopoulos, R Canal, et al.	2D error correction for F/F based arrays using In-Situ Real-Time Error Detection (RTD)	2020	DFT
4	A Lasheras, R Canal, E Rodríguez, L Cassano	Lightweight protection of cryptographic hardware accelerators against differential fault analysis	2020	IOLTS
4	M Fusi, F Mazzocchetti, A Farres, L Kosmidis, R Canal, et al.	On the use of probabilistic worst-case execution time estimation for parallel applications in high performance systems	2020	Mathematics
0	N Gutiérrez, E Rodríguez, S Mus, B Otero, R Canal	Privacy preserving Deep Learning framework in Fog computing	2020	LOD

0	A Bosio, R Canal, S Di Carlo, D Gizopoulos, A Savino	Cross-Layer Soft-Error Resilience Analysis of Computing Systems	2020	DSN
8	G Agosta, W Fornaciari, D Atienza, R Canal, et al.	Challenges in deeply heterogeneous high performance systems	2019	Euromicro (DSD)
1	A Lasheras, R Canal, E Rodríguez, L Cassano	Protecting RSA hardware accelerators against differential fault analysis through residue checking	2019	DFTS
25	A Vallero, et al.	Syra: Early system reliability analysis for cross-layer soft errors resilience in memory arrays of microprocessor systems	2018	IEEE Transactions on Computers
5	M Anglada, R Canal, JL Aragon, A González	Fast and accurate SER estimation for large combinational blocks in early stages of the design	2018	IEEE Transactions on Sustainable Computing
4	E Amat, R Canal, A Rubio	Modem gain-cell memories in advanced technologies	2018	IOLTS
2	J Verdu, JJ Costa, B Otero, E Rodriguez, A Pajuelo, R Canal	Platform-Agnostic Steal-Time Measurement in a Guest Operating System	2018	arXiv preprint
0	E Amat, A Calomarde, R Canal, A Rubio	Optimization of FinFET-Based Gain Cells for Low Power Sub-V T Embedded DRAMs	2018	Journal of Low Power Electronics
0	E Amat, R Canal Corretger, A Calomarde Palomino, JA Rubio Sola	Review on suitable eDRAM configurations for next nano-metric electronics era	2018	International journal of Materials Engineering
47	M Kaliorakis, D Gizopoulos, R Canal, A Gonzalez	Merlin: Exploiting dynamic instruction behavior for fast and accurate microarchitecture level reliability assessment	2017	ISCA
3	M Rana, R Canal, E Amat, A Rubio	Statistical analysis and comparison of 2T and 3T1D e-DRAM minimum energy operation	2017	IEEE Trans. on Device and Materials Reliability