Ramon Canal
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Education: 2006-2007 Visiting Scholar. Harvard University (Cambridge, MA, USA).
2004 PhD at the Department of Computer Architecture at UPC.
Advisors: J. E. Smith (U. of Wisconsin-Madison, USA), A. González (UPC).
1998: MSc in Computer Science Engineering, UPC.
Final year done at the University of Bath, UK.

Key figures:

Publications (Peer reviewed)	>60
Total citations	>1300
H-index	17
G-index	36
Cites/year	74

Invited talks/Keynotes	22
Awards	9
Projects (PI)	4
Projects (Key personnel/coordinator)	3
Scientific Committees	23

Current positions:
2008 – now Associate Professor, Barcelona School of Informatics, UPC, Spain
2013 – 2017 Vice dean of Postgraduate Studies, Barcelona School of Informatics, UPC, Spain.

Previous positions:
2006 – 2007 Visiting Scholar, Harvard University, Cambridge (Massachusetts), USA.
2003 – 2008 Assistant Professor, Barcelona School of Informatics, UPC, Spain
2003 – 2006 Invited Lecturer, School of Engineering, Universitat Ramon Llull (URL), Spain
2000/6–2000/10 Intern, Sun Microsystems, Sunnyvale (California), USA.

Fellowships:
2006-2007 Fulbright Award. Visiting Scholar at Harvard University (Fulbright association). (40,000€)
2000-2003 PhD fellowship, Generalitat de Catalunya (government), Spain (50,000€)

Graduated PhD Students (under my supervision) (19) (first job in brackets):
- 4 PhD students: Matteo Monchiero (HP Labs), Enric Herrero (Intel Labs), Shrikanth Ganapathy (EPFL Switzerland), Zoran Jaksic (Broadcom)
- 15 Master students.

Current PhD Students (under my supervision) (2) (expected graduation in brackets):
- 2 PhD students: Josué Quiroga (‘19), Octavio Campo (’20)

Honors and Awards (10+3):
2016 Senior Member of the IEEE (2016)
2013 Recognition for Excellence in Education (2008-2012, evaluation every 5 years) UPC, AQU Catalunya
2010 Recognition for Excellence in Education (2003-2007, evaluation every 5 years) UPC, AQU Catalunya
2008 First price in the 6th Duran Farell Award on technology and research in Spain, UPC and Gas Natural, member of the research team of the project: "Efficient processor design through clustering”
2001 First Price in the Epson Foundation Rosina Ribalta Award to the best thesis project in the area of Information Technologies in Spain and Portugal, 2001

5 Paper Awards: Best Paper (DCIS '12, HPCA '00), Best paper nominee (ICCD '14), HiPEAC Award ('10), IEEE Micro Top Picks ('08)

As an advisor, my students have received the following awards:
2014 Intel Doctoral Student Programme Honoree (Zoran Jaksic-PhD student, 35,000$)
2013 Outstanding PhD Award in the ICT area. UPC. (Dr. Enric Herrero)
2012 Intel Doctoral Student Programme Honoree (Shrikanth Ganapathy -PhD student, 35,000$)

Organisation of scientific meetings (3)

2016	General co-chair. IEEE/ACM Int. Symp. on High Performance Computer Arch.(HPCA), Barcelona (Spain), February 2016, 250 participants.
2014	Students chair, IEEE/ACM International Symposium on Code Generation and Optimization, February 2014, Orlando (FL-USA), 120 participants.
2012	General co-chair IEEE On-Line Testing Sympiosum (IOLTS), Sitges (Spain), June 2012. 70 participants.

Commissions of trust

2016 – now	Associate Editor Journal of Parallel and Distributed Computing, Elsevier.
2009, 2010	Scientific Advisory Board, Fulbright Award selection committee in Spain.
2009	Evaluator, Nederlandse Organisatie voor Wetenschappelijk Onderzoek - Netherlands Organisation for Scientific Research (NWO).

Program committee member (selection of 11 highest ranked conferences)

'11 '13 '17	IEEE/ACM International Symposium on Computer Architecture (ISCA)
'17	IEEE International Symposium on Microarchitecture (MICRO)
'12 '13 '14	IEEE/ACM International Symposium on High Performance Computer Architecture (HPCA)
'08 '10 '16 '17	IEEE International Conference on High Performance Computing (HiPC)
'09 '14 '17	International Conference on Parallel Processing (ICPP)
'09 '14 '17	IEEE International Parallel & Distributed Processing Symposium (IPDPS)
'16	IEEE Micro Top Picks
'14 '16	IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)
'13 '14	IEEE/ACM Conference on Supercomputing (SC)
'06 '08	IEEE International Conference on Computer Design, Lake Tahoe (ICCD)
'06 '07	International Conference on Parallel and Distributed Systems (ICPADS)

Board of Reviewers

2000 – now	Regularly in IEEE and ACM conferences and journals such as: ISCA, MICRO, HPCA, ASPLOS, PACT, ICS, EUROPAR, CGO, IPDPS, ICPADS, ICCD, Hipeac, IEEE Micro, IEEE Micro Top Picks, IEEE Transactions on Computers, IEEE Transaction on VLSI Systems, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Evolutionary Computing, IET Circuits, Devices & Systems, ACM Transactions on Architecture and Code Optimization, Journal of Systems Architecture.

Keynotes/Panels/Seminars (5):

- "Big Data to wearables, a hardware perspective", seminar at the Faculty of Pure and Applied Sciences, University of Cyprus, April 2015.
- "The memory hierarchy in the many-core era: friend or foe?" Keynote at 1st International Workshop on On-chip Memory Hierarchies and Interconnects (OMHI). Europar-2012. Rhodes (Greece), August 2012
- "Compensation Mechanisms at Digital Circuit Design Level" Keynote at the 3rd European Workshop on CMOS Variability (VARI 2012), Nice (France), June 2012
- "Challenges in Computing in the Age of Heterogeneous Platforms" Panel member at the XXIX IEEE International Conference of Computer Design (ICCD 2011), Amherst (MA, USA), October 2011
- "Low Power Microarchitectures, tools for power/reliability simulation/estimation" Seminar at École thématique ARCHI'11, Mont-Louis (France), June 2011

Invited talks (17):

- "Memory Organization in the Multi/Many-Core Era" Invited talk at Intel Microprocessor Technology Lab, Hillsboro (OR-USA), January 2016
- "Memory Organization in the Multi/Many-Core Era" Invited talk at Intel Microprocessor Research Lab, Bangalore (India), November 2015

- "The Uncertainty of Technology and its Consequences", invited talk at the Error-Aware Systems: Opportunities and Challenges for Handling Errors at Multiple Levels track in the Hipeac Computer Systems Week. Athens (Greece), October 2014
- "Reliability in High Performance Computing, peanuts or hot potato?" Invited talk at the IEEE International On-Line Testing Symposium (IOLTS 2014), Platja d'Aro (Spain), July 2014
- "FinFETs and their impact on SRAM and DRAM memories", FP7 Variability and Reliability Showcase, held in the ESSCIRC/ESSDERC 2013. Bucharest (Romania), September 2013
- "New cells and reliability mechanisms for next generation memories", CASTNESS'13, Computing Architectures Software tools and nano-Technologies. For Numerical Embedded and Scalable Systems. Barcelona (Spain), June 2013
- "Challenges and opportunities in memory research in the FinFET and many-core era", Shanghai Jiao Tong University, China, February 2013
- "Are FinFETs the panacea?",Workshop The intertwining challenges of reliability, testing and verification. Held in the Hipeac Systems Week 2012. Ghent (Belgium), October 2012
- "FinFET Technology for Memories: Pros and Cons" IEEE International On-Line Testing Symposium (IOLTS 2012), Sitges (Spain), June 2012
- "TRAMS: peeking into the future of technology and systems" TF on reliability at HiPEAC Spring Computing Systems Week, Chamonix (France), April 2011
- "Memory Organization in the Multi/Many-Core Era", Intel Microprocessor Technology Lab, Hillsboro (OR-USA), February 2011
- "Run-time PVT variations monitoring and adaptation", Intel Circuit Research Lab, Hillsboro (OR-USA), February 2011
- "Reliability: the next big challenge", Universitat PolitècnicaValència (Spain), November 2010
- "Future trends and challenges in the microprocessor world", U. del Turabo, Puerto Rico, 2/3/2007
- "Future trends and challenges in the microprocessor world", U. Metropolitana, Puerto Rico, 2/3/2007
- "Computer architecture research by the Mediterranean", Department of Electrical and Computer Engineering, Harvard University, Cambridge (MA-USA), 25/10/2006
- "How to keep cool and get the job done", NU Computer Architecture Research Group, Northeastern University, Boston (MA-USA), 29/6/2006

Membership of scientific societies

2004 – now	Member, Research Network of Excellence (UE) "*Hipeac*", UE
2002 – now	Member of the IEEE Computer Society. Senior Member since 2016. Worldwide.
2002 – now	Member of the ACM and ACM SIGARCH interest group. Worldwide.
2000 – now	Funding member of the Spanish Society of Computer Architecture and Technology (SARTECO), Spain
1999 – now	Member of the Official College of Computer Science Engineers of Catalonia (COEIC), Catalonia, Spain

Major collaborations

- Prof. Xiaoyao Liang, GPU memory hierarchy and variability, Shanghai Jiao Tong University, China.
- Prof. Dimitris Gizopolous, Reliability in multicore CPUs and memories, University of Athens, Greece.
- Prof. David Brooks, DRAM memories, Harvard University, Cambridge-Massachusetts, USA.
- Dr. Dan Alexandrescu, Reliability modelling and analysis, iROC Technologies, France.
- Prof. Bruce Cockburn, Statistical modeling of reliability, University of Alberta, Edmonton, Canada

Standard part of the curriculum in graduate level courses of my works (11):

The courses (outside Spain) that list (or have listed) my papers are (info taken from each course webpage):

- Massachusetts Institute of Technology (MIT) (USA): 6.375 Complex Digital Systems
- University of Michigan (USA): EECS 573: Microarchitecture
- University of Illinois at Urbana-Champaign (USA): ECE 512: Microarchitecture
- University of California-San Diego(USA):CSE291:Topics on High-Performance Processor Architectures
- University of Utah (USA): CS7960-4 and CS 7937 / 7940 High-Performance Architectures
- University of Pittsburg (USA): CS2410 - Computer Architecture
- State University of NewYork at Binghamton(USA):CS-580a Advanced Topics in Computer Architecture
- Rice University (USA) COMP 522: Multi-core Computing
- University of Nebraska – Lincoln (USA): CSCE930: Advanced Computer Architecture

- University of Maryland (USA): ENEE 698B: Computer Engineering Seminar
- University of Edinburgh (Scotland): Energy Aware Computing
- TU Delft (The Netherlands): ET4-074: Modern Computer Architectures

Participation in projects

Industry international

2013-2015 PI. Cache Design in the Finfet Era. Intel corporation 35000$

2012-2014 PI. Reliability in the face of variability in the nanometer era. Intel corporation 35000$

2000-2001 Research staff. The subscalar microarchitecture. IBM Corporation. 40000$

Public Administration. EU.

2014-2016 Key Personnel. Cross-Layer Early Reliability Evaluation for the Computing Continuum (CLERECO), FP7-611404 (2555000€)

2010-2012 Key Personnel. Terascale Reliable Adaptive Memory System (TRAMS), FP7-248789 (2400000€)

2005-2007 Coordinator. HW/SW Parallelism Exploitation in Chip Multiprocessor Architectures", Spanish Ministry of Education and Science – Italian Ministry of Science and Technology, HI2005-0299 (11040€)

1998-1999 Research Staff. Memory Hierarchy Analysis and Optimization Tools for the End-User (MHAOTEU), European Union, RTD project number 24942 (1000000 ECUS)

Public Administration. Spain.

2014-2016 Sub-group Leader. "Microarquitectura y compiladores para futuros procesadores 3", Spanish Ministry of Economy, TIN2013-44375-R (333283€)

2011-2013 Sub-group Leader. "Arquitecturas y Compiladores 3", Spanish Ministry of Science and Technology, TIN2010-18368 (242242€)

2011-2013 Member."Red Española de Variabilidad en Tecnologías, circuitos y sistemas micro/nanoelectrónicos", Spanish Ministry of Economy and Competitiveness", TEC2011-15599-E

2008-2011 Sub-group Leader. "Arquitecturas y Compiladores 2", Spanish Ministry of Education and Science, TIN2007-61763. (276.000€)

2008-2011 Member . "Computación de Altas Prestaciones IV: Arquitecturas, Compiladores, Sistemas Operativos, Herramientas y Aplicaciones", Spanish Ministry of Education and Science, TIN2004-07739-C02-01. (1.190.000€)

2008-2011 Member. ""Computación de Altas Prestaciones III: Arquitecturas, Compiladores, Sistemas Operativos, Herramientas y Algoritmos", Spanish Ministry of Education and Science, TIC2001-0995-C02-01. (1.161.564€)

2008-2011 Member. "Computación de Altas Prestaciones II: Arquitecturas, Compiladores, Sistemas Operativos y Aplicaciones", Spanish Ministry of Education and Science, TIC98-0511. (109060000pts)

2009-2013 Sub-group leader. "Microarquitectura i Compiladors", Generalitat de Catalunya, Agencia de Gestió d'Ajuts Universitaris i de Recerca, 2009SGR1250. (46.800€)

2005-2009 Sub-group leader. "Arquitectures i Compiladors", Generalitat de Catalunya, Agencia de Gestió d'Ajuts Universitaris i de Recerca, 2005SGR00950. (37.600€)

Institutional Responsibilities

2013 – now Vice dean of Postgraduate Studies, Barcelona School of Informatics, UPC, Spain.

2010 – 2013 Coordinator of the Undergraduate Computer Engineering Curricula, Barcelona School of Informatics, UPC, Spain

2008 – 2011 Secretary of the Department of Computer Architecture, UPC, Spain

2007 – 2010 Member of the New Computer Science Curricula Committee,, UPC, Spain

Teaching activities

2012 – now Master courses in Processor Design and Nanotechnology Circuit Design, Barcelona School of Informatics, UPC, Spain

2003 – 2011 Master and Bachelor courses on Computer Architecture and Microprocessor Design, Barcelona School of Informatics, UPC, Spain

Publications (H-index = 17, G-index = 36, Total refs: >1300):

The Computer Architecture community strongly depends on short turn-around times. Thus, publishing in a conference has a higher impact than in a journal and conferences include both the publication of the work (usually 10-pages) and a presentation of the work (30 minutes). Moreover, the selection process is peer-reviewed in both cases and acceptance rates are around 10%-25%. The classification the conferences is extracted from: http://www.conferenceranks.com/. All the papers listed are in the top peer reviewed conferences in the area.

Journals (all peer-reviewed)

		Impact (JCR[1]-quartile)	Impact (Core 2017)	Citations (google scholar)
17	"Statistical Analysis and Comparison of 2T and 3T1D e-DRAM Minimum Energy Operation", M.Rana, R. Canal, E. Amat, A. Rubio, IEEE Transactions on Device and Materials Reliability v17 n1 pp. 42-51	1,575 – Q3	N/A	-
16	"Feasibility of the embedded DRAM cells implementation with FinFET devices", E. Amat, A. Colomarde, F. Moll, R. Canal, A. Rubio IEEE Transactions on Computers v.65 n.4, pp. 1068-1074, April 2016	1,723 – Q1	A*	2
15	"Variability Influence on FinFET-based On-chip Memory Data Paths" E. Amat, A. Colomarde, F. Moll, R. Canal, A. Rubio Journal of Low Power Electronics v. 11, n. 2, June 2015	N/A	N/A	-
14	"Strategies to enhance the 3T1D-DRAM cell variability robustness beyond 22nm", E. Amat, C.G. Almudéver, N. Aymerich, R. Canal, A. Rubio, Microelectronics Journal v. 45, n. 10, pp. 1342–1347, October 2014	0,836 – Q3	N/A	1
13	"Suitability of the FinFET 3T1D cell beyond 10nm", E. Amat, C.G. Almudéver, N. Aymerich, R. Canal, A. Rubio, IEEE Transactions on Nanotechnology v.13, n.5, pp.926-932, September 2014	1,825 – Q2	N/A	1
12	"Impact of FinFET and III-V/Ge technology on logic and memory cell behavior" E. Amat, A. Calomarde, C.G. Almudever, N. Aymerich, R. Canal, A. Rubio IEEE Transactions on Device and Materials Reliability v.14, n. 1, pp. 344 - 350, March 2014	1,890 – Q2	N/A	8
11	"Variability mitigation mechanisms in scaled 3T1D DRAM memories to 22nm and beyond"; E. Amat, C.G. Almudever, N. Aymerich, R. Canal, A. Rubio; IEEE Transactions on Device and Materials Reliability v.13, n.1, pp. 103-109, March 2013	1,544 – Q2	N/A	9
10	"Comparison of SRAM Cells for 10-nm SOI FinFETs Under Process and Environmental Variations", Z. Jakšić, R. Canal, IEEE Transactions on Electron Devices, v.60 n.1 pp. 49-55 , January 2013	2,476 – Q1	N/A	7
9	"Impact of FinFET technology introduction in the 3T1D-DRAM memory cell"; E. Amat, C.G. Almudever, N. Aymerich, R. Canal, A. Rubio; IEEE Transactions on Device and Materials Reliability, 2013	1,544 – Q2	N/A	4
8	"Thread Row Buffers: Improving memory performance isolation and throughput in multiprogrammed environments"; E. Herrero, J. González, R. Canal, D. Tullsen; IEEE Transactions on Computers v. 62 n. 9 pp. 1879-1892, 2013.	1,473 – Q2	A*	10
7	"Distributed Cooperative Caching: An Energy Efficient Memory Scheme for Chip Multiprocessors"; E. Herrero, J. González, R. Canal; IEEE Transactions on Parallel and Distributed Systems, v. 23, n. 5, pp. 853-861, May 2012.	1,796 – Q1	A*	14
6	"Impact of Positive Bias Temperature Instability (PBTI) on 3T1D-DRAM Cells"; N. Aymerich, S. Ganapathy, A.Rubio, R. Canal, A. González; Integration, the VLSI Journal v.45 n. 3 pp. 246-252. December 2011.	0,414 – Q4	N/A	6
5	"Power/Performance/Thermal Design Space Exploration for Multicore Architectures", M. Monchiero, R. Canal, A. González, IEEE	1,916 – Q1	A*	74

[1] Journal Citation Record in the year of publication

	Transactions on Parallel and Distributed Systems v19. n. 5 pp. 666-681, March, 2008.			
4	"Replacing 6T SRAMs with 3T1D DRAMs in the L1 Data Cache to Combat Process Variability", X. Liang, R. Canal, G.Y. Wei, D. Brooks, IEEE Micro v.28 n.1 pp. 60-68 Micro's Top Picks from Computer Architecture Conferences, Jan/Feb 2008	2.565 – Q1	N/A	45
3	"Value Compression for Efficient Computation", R. Canal, A. González and James E. Smith, Lecture Notes in Computer Science, v. 3648, pp. 519-529, Springer-Verlag, 2005.	N/A	N/A	2
2	"Power- and Complexity-Aware Issue Queue Designs", J. Abella, R. Canal and A. González, IEEE Micro Special Issue on Power- and Complexity-Aware Design, September-October 2003	1,059 – Q2	N/A	34
1	"Dynamic Code Partitioning for Clustered Architectures", R. Canal, J.M. Parcerisa and A. González, International Journal of Parallel Processing, vol 29 n. 1, 2001.	0,154 – Q4	N/A	28

	Conferences (all peer-reviewed)		(Core 2017 – Qualis)	
40	"MeRLiN: Exploiting Dynamic Instruction Behavior for Fast and Accurate Microarchitecture Level Reliability Assessment". M. Kaliorakis, D. Gizopoulos, R. Canal, A. González. ACM/IEEE International Conference on Computer Architecture (ISCA 2017), June 2017		A*-A1	
39	"Cross-Layer System Reliability Assessment Against Hardware Faults", A. Vallero, A. Savino, G. Politano, S. Di Carlo, A. Chatzidimitriou, S. Tselonis, M. Kaliorakis, D. Gizopoulos, M. Riera, R. Canal, A. Gonzalez, M. Kooli, A. Bosio, G. Di Natale, IEEE International Test Conference (ITC-47), Fort Worth (TX, USA), November 2016		B-A1	
38	"SRAM Memory Margin Probability Failure Estimation using Gaussian Process Regression ", M. Rana, R. Canal, J. Han and B. Cockburn, IEEE International Conference on Computer Design (ICCD-34), Phoenix (AZ, USA), October 2016		N/A-A2	
37	"MASkIt: Soft Error Rate Estimation for Combinational Circuits", M. Anglada, R. Canal, J. L. Aragón and A. González, IEEE International Conference on Computer Design (ICCD-34), Phoenix (AZ, USA), October 2016		N/A-A2	
36	"Statistical Analysis and Comparison of 2T and 3T1D e-DRAM Minimum Energy Operation", M.Rana, R.Canal, E.Amat, A.Rubio, 22th IEEE International On-Line Testing Symposium (IOLTS'16), St. Feliu de Guíxols (Spain), July 2016		C-B1	
35	"A Detailed Methodology to Compute Soft-Error Rates in Advanced Technologies", M. Riera, R. Canal, J. Abella. A. Gonzalez, IEEE Design, Automation and Test in Europe Conference (DATE'16), Dresden (Germany), March 2016		B-A1	2
34	"Variability - Aware Design Space Exploration Of Embedded Memories", S. Ganapathy, G. Karakonstantis, A. Burg and R. Canal, IEEE 28th Convention of Electrical and Electronics Engineers in Israel, Eilat (Israel), December 2014		N/A	5
33	"REEM: Failure/Non-Failure region Estimation method for SRAM yield analysis", M. Rana, R. Canal, IEEE International Conference on Computer Design (ICCD-32), Seoul (Korea), October 2014		N/A-A2	
32	"iRMW: A Low-Cost Technique to Reduce NBTI-Dependent Parametric Failures in L1 Caches" (Best paper nomenee), S. Ganapathy, R. Canal, A. González and A. Rubio, IEEE International Conference on Computer Design (ICCD-32), Seoul (Korea), October 2014		N/A-A2	2
31	"Variability impact on on-chip memory data paths", E. Amat, A. Calomarde, R. Canal, A. Rubio, IEEE European Workshop on CMOS Variability (VARI'14), Palma de Mallorca (Spain), September 2014		N/A	1

30	"SSFB: A Highly-Efficient and Scalable Simulation Reduction Technique for SRAM Yield Analysis", M. Rana, R. Canal, IEEE Design, Automation and Test in Europe Conference (DATE'14), Dresden (Germany), March 2014		B-A1	2
29	"DRAM-based Coherent Caches and how to take advantage of the coherence protocol to reduce the refresh power", Z. Jakšić, R. Canal IEEE Design, Automation and Test in Europe Conference (DATE'14), Dresden (Germany), March 2014		B-A1	2
28	"INFORMER: An Integrated Framework for Early-Stage Memory Robustness Analysis", S. Ganapathy, R. Canal, D. Alexandrescu, E. Costenaro, A. González and A. Rubio, IEEE Design, Automation and Test in Europe Conference (DATE'14), Dresden (Germany), March 2014		B-A1	4
27	"Variability Robustness Enhancement for 7nm FinFET 3T1D-DRAM Cells ", E. Amat, C.G. Almudéver, N. Aymerich, R. Canal, A. Rubio, IEEE 56th International Midwest Symposium on Circuits and systems (MWSCAS 2013) Columbus (Ohio, USA), August 2013		N/A-B1	1
26	"An Energy-Efficient and Scalable eDRAM-Based Register File Architecture for GPGPU", N. Jing, Y. Shen, Y. Lu, S. Ganapathy, Z. Mao, M. Guo, R. Canal, X. Liang, ACM/IEEE International Conference on Computer Architecture (ISCA'13), Tel-Aviv (Israel), June 2013		A*-A1	39
25	"Combining RAM technologies for hard-error recovery in L1 data caches working at very-low power modes"; V. Lorente, A. Valero, J. Sahuquillo, S. Petit, R. Canal, P. Lopez, J. Duato; IEEE Design, Automation and Test in Europe Conference (DATE'13), Grenoble (France), March 2013		B-A1	7
24	"On the Effectiveness of Hybrid Recovery Techniques on Parametric Failures"; S. Ganapathy, R. Canal, A. González, A. Rubio; 30th IEEE International Symposium on Quality Electronic Design (ISQED'13), Santa Clara (California, USA), March 2013		N/A-B1	4
23	"Enhancing 3T DRAMs for SRAM replacement under 10nm Tri-Gate SOI FinFETs"; Z. Jakšić, R. Canal; 30th IEEE International Conference on Computer Design (ICCD'12), Montreal (Quebec), September 2012		N/A-A2	2
22	"A Novel Variation-Tolerant 4T-DRAM with Enhanced Soft-Error Tolerance"; S. Ganapathy, R. Canal, D. Alexandrescu, E. Costenaro, A. González, A. Rubio; 30th IEEE International Conference on Computer Design (ICCD'12), Montreal (Quebec), September 2012		N/A-A2	11
21	"Analysis of FinFET Technology on Memories" (invited paper); E. Amat, A. Asenov, R. Canal, B. Cheng, J-L. Cruz, Z. Jakšić, M. Miranda, A. Rubio, P. Zuber; 18th IEEE International On-Line Testing Symposium (IOLTS'12), Sitges (Spain), June 2012		C-B1	-
20	"Enhancing 6T SRAM cell stability by back gate biasing techniques for10nm SOI FinFETs under process and environmental variations", Z. Jaksic, R. Canal, Proceedings of the 19th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES 2012, Warsaw, 2012, pp. 103-108.		N/A	11
	"Impact of bulk/SOI 10nm FinFETs on 3T1D-DRAM cell performance", E. Amat, C. Almudéver, N. Aymerich, R. Canal, A. Rubio, IEEE 11th International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Xian (China) 2012			
	"Strain relevance on the improvement of the 3T1D cell performance", E. Amat, C. Almudéver, N. Aymerich, R. Canal, A. Rubio, Proceedings of the 19th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES 2012, Warsaw, 2012, pp. 120-123.		N/A	
19	"Dynamic Fine-Grain Body Biasing of Caches with Latency and Leakage 3T1D-Based Monitors"; S. Ganapathy, R. Canal, A. González, A. Rubio; 29th IEEE International Conference on Computer Design		N/A-A2	4

	(ICCD'11), Amherst (MA, USA), October 2011			
18	"New reliability mechanisms in memory design for sub-22nm technologies" (invited paper); N. Aymerich, A. Asenov, A. Brown, R. Canal, B. Cheng, J. Figueras, A. González, E. Herrero, S. Markov, M. Miranda, P. Pouyan, T. Ramirez, A. Rubio, I. Vatajelu, X. Vera, X. Wang, P. Zuber; 17th IEEE International On-Line Testing Symposium (IOLTS'11), Athens (Greece), July 2011		C-B1	7
17	"Impact of Positive Bias Temperature Instability (PBTI) on 3T1D-DRAM Cells"; N. Aymerich, S. Ganapathy, A.Rubio, R. Canal, A. González; 21st ACM Great Lakes Symposium on VLSI, Lausanne (Switzerland), May 2011		N/A-B1	6

16	"MODEST : A Model for Energy Estimation under Spatio-Temporal Variability"; S. Ganapathy, R. Canal, A. González, A. Rubio; 15th ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED 2010) , August 2010 (Austin, Texas)		N/A-A1	4
15	"Circuit Propagation Delay Estimation Through Multivariate Regression-Based Modeling Under Spatio-Temporal Variability"; S. Ganapathy, R. Canal, A. González, A. Rubio; IEEE Design, Automation and Test in Europe Conference (DATE'10), March 2010 (Dresden, Germany)		B-A1	23
14	"Power-Efficient Spilling Techniques for Chip Multiprocessors"; E. Herrero, J. González, R. Canal; International Conference on Parallel Computing, (EURO-PAR'10), Ischia (Italy), September 2010		A-A2	9
13	"Elastic Cooperative Caching: An Autonomous Dynamically Adaptive Memory Hierarchy for Chip Multiprocessors "; Enric Herrero, José González, Ramon Canal; IEEE 37th International Conference on Computer Architecture (ISCA'10), Saint-Malo (France), June 2010		A*-A1	67
12	"An hybrid eDRAM/SRAM macrocell to implement first-level data caches ", A. Valero, J. Sahuquillo, S. Petit, V. Lorente, R. Canal, P. Lopez, J. Duato; IEEE/ACM International Symposium on Microarchitecture (MICRO-42), New York (New Jersey); Dec. 2009		A-A1	37
11	"Using Coherence Information and Decay Techniques to Optimize L2 Cache Leakage in CMPs", M. Monchiero, R. Canal, A. González IEEE 38th International Conference on Parallel Processing (ICPP), Vienna (Austria), September 2009		A-A2	10
10	"Distributed Cooperative Caching", E. Herrero, J. González, R. Canal, IEEE/ACM 17th International Conference on Parallel Architectures and Compilation Techniques (PACT), Toronto (CA), Oct. 2008.		A-A2	59
9	"Process Variation Tolerant 3T1D-Based Cache Architectures", X. Liang, R. Canal, G.Y. Wei, D. Brooks, IEEE/ACM Int. Symposium on Microarchitecture (MICRO-40), Dec. 2007 (Chicago, USA)		A-A1	102
8	"Design Space Exploration for Multicore Architectures: A Power/Performance/Thermal View", M. Monchiero, R. Canal, A. González, ACM International Conference on Supercomputing (ICS-06), Cairns (Australia), June 2006.		A-A2	98
7	"Value compression for efficient computation", R. Canal, A. González, J. E. Smith; Int. Conference on Parallel Computing, (EURO-PAR'05), Lisboa (Portugal), August 2015		A-A2	3
6	"Software-Controlled Operand-Gating", R. Canal, A. González, James E. Smith, IEEE/ACM 2004 International Symposium on Code Generation and Optimization, Palo Alto (CA), March 2004.		A-A2	25
5	"Reducing the Complexity of the Issue Logic", R. Canal, A. González, ACM International Conference on Supercomputing (ICS-01), Sorrento (Italy), June 2001.		A-A2	71
4	"Very Low Power Pipelines using Significance Compression", R. Canal, A. González, J. E. Smith, IEEE/ACM Int. Symposium on Microarchitecture (MICRO-33), Monterey (CA) Dec. 2000.		A-A1	138
3	"A Low-Complexity Issue Logic", R. Canal, A. González. ACM International Conference on Supercomputing (ICS-00), Santa Fe (NM), May 2000.		A-A2	112
2	"Dynamic Cluster Assignment Mechanisms", R. Canal, J.M. Parcerisa and A. González, IEEE/ACM Int. Symposium on High Performance Computer Architecture (HPCA-6), Toulouse, Jan. 2000.		A*	147
1	"A Cost-Effective Clustered Architecture", R. Canal, J.M. Parcerisa and A. González, IEEE/ACM 8th International Conference on Parallel Architectures and Compilation Techniques (PACT), Newport Beach, Oct. 1999.		A-A2	74

Book chapter

1	Jichuan Chang, Enric Herrero, Ramon Canal and Gurindar S. Sohi. "Cooperative Caching for Chip Multiprocessors". In "Cooperative Networking" (Chapter13), John Wiley & Sons, July 2011. ISBN: 978-0-470-74915-9.			

Posters, Workshops or non-index journals

7-1	Other conferences and workshops: DCIS, ICSICT, MIXDES, ASGI Other journals: Procedia Computer Science Posters: Intel ERIC			1
			TOTAL NUMBER OF CITATIONS (Google Scholar) :	**>1300**

Other:

- Editorial Pearson Educación/Prentice Hall (2006) evaluation of the book to determine the impact in graduate level courses at Spanish universities. "Microprocesadores Intel: arquitectura, programación e interfaz.", séptima edición, Barry B. Brey, Pearson Educación/Prentice Hall, ISBN: 970-26-084-X
- Editorial Reverté (2005) evaluation of the book to determine the impact of a translation. "Computer Organization and Design. The Hardware/Software interface", J.L. Hennessy y D.A. Patterson, Morgan-Kaufman, 2004, ISBN: 978-1-55860-604-3
- Member of the translation team of the book "Computer Organization and Design. The Hardware/ Software interface" of L.L. Hennessy and D.A. Patterson from English to Spanish ("Estructura y diseño de computadores. Interfície Circuitería/Programación", ISBN 84-291-2616-3), 1998.