Power and Complexity Aware Microarchitectures

Jaume Abella[1]

jabella@ac.upc.es

http://people.ac.upc.es/jabella

Ramon Canal[1]

rcanal@ac.upc.es

http://people.ac.upc.es/rcanal

Antonio González[1,2]

antonio@ac.upc.es

http://people.ac.upc.es/antonio

[1] Computer Architecture Dept. UPC-Barcelona

[2] Intel-UPC Barcelona Research Barcelona, Spain

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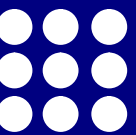
Issue Logic (I)

- **Adaptive IQ**
  - Resize dynamically the ROB and issue queue according to their occupancy

    "Power-Aware Adaptive Issue Queue and Register File", HiPC 2003
- **Dependence Based IQ**
  - Keep direct relationships between producer and consumer

    "Reducing the Complexity of the Issue Logic", ICS 2001
- **Prescheduling IQ**
  - Schedule instruction issue according to the latencies of functional units

    " A Low Complexity Issue Logic", ICS 2000



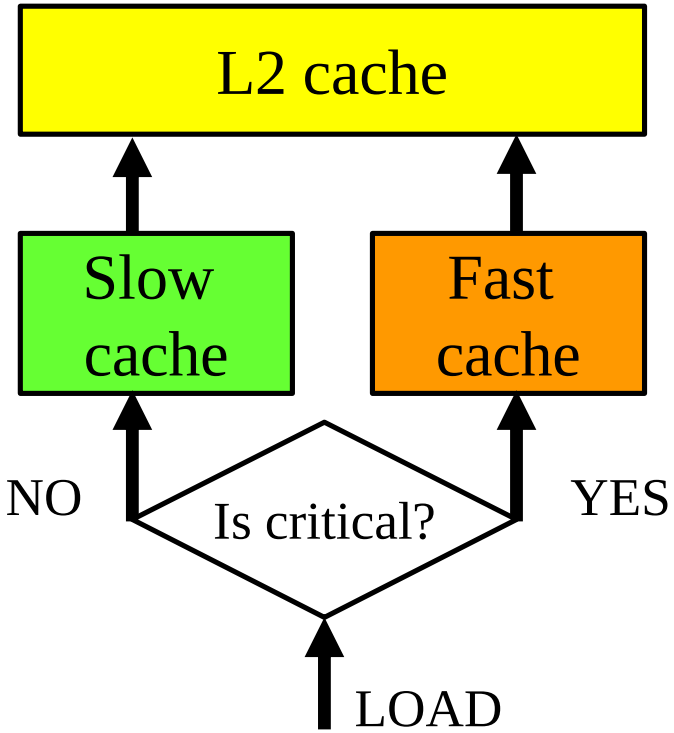
Issue Logic (II)

- **FP distributed issue queue without CAM cells**
  - Dispatch
    - Instructions belonging to a dependence chain are sent to the same queue
    - Multiple dependence chains may share a queue
  - Issue
    - Small table keeps track of how many cycles has to wait the first instruction of a chain to be issued
    - First, select the oldest instruction that will become ready next cycle. Second, the oldest ready instruction

"Low-Complexity Distributed Issue Queue", HPCA 2004

Memory Hierarchy

Heterogeneous L1 Dcache banks



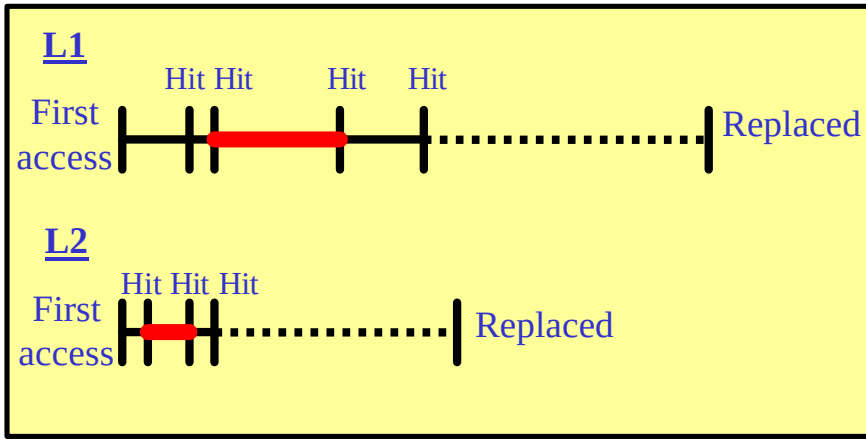
"Power Efficient Data Cache Designs", ICCD 2003

Adaptative L2 Cache

Shutdown Cache Lines

Current predictors are L1 cache oriented

L1 and L2 behave quite different



Access counts and inter-access time are used to compute decay intervals

"Smart Predictors to Turn-off L2 Cache Lines", under submission

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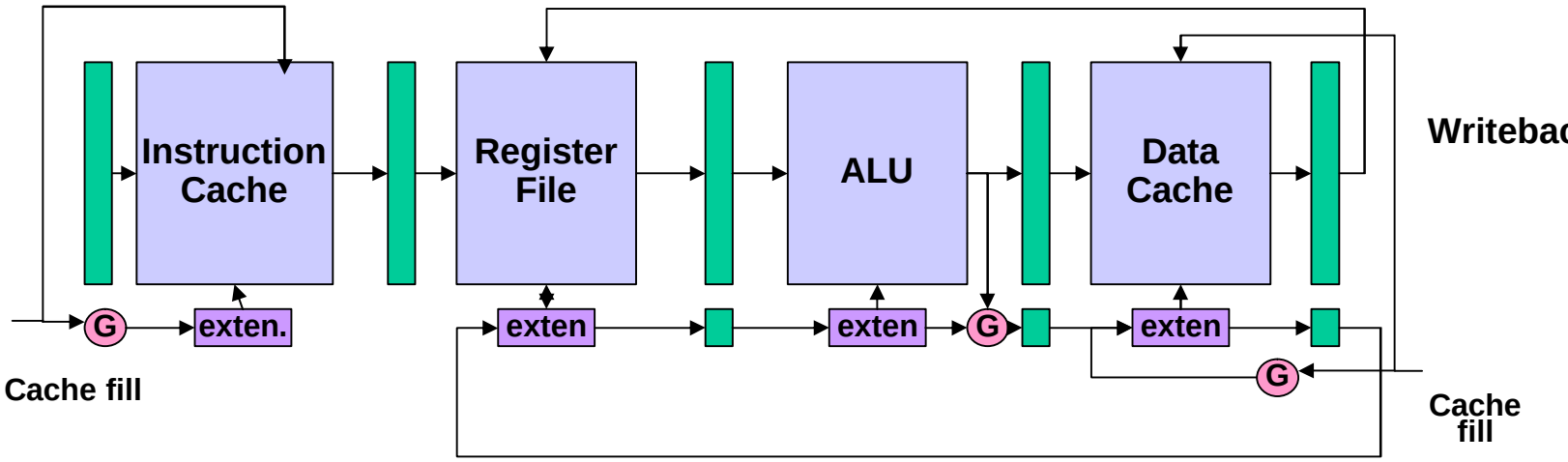
Hw Value Compression

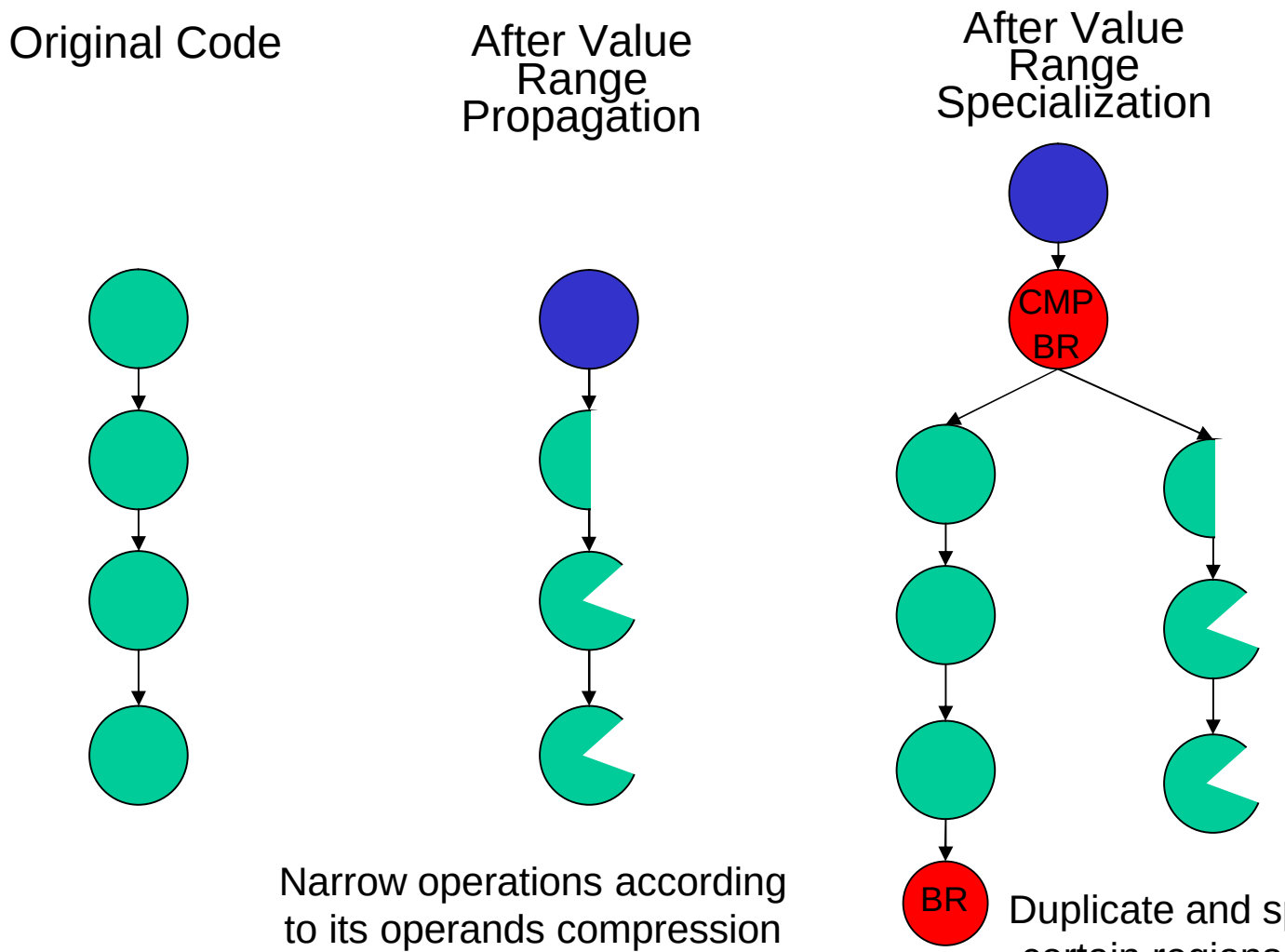


32-bit embedded processor pipeline with value compression

- **Dynamically compress values flowing through the pipeline**
- **Good for embedded and high performance processors!!**

"Very Low Power Pipelines using Significance Compression", MICRO-33

Compiler directed Value Compression



"Software-Controlled Operand-Gating", CGO 2004