Design Space Exploration for Multicore Architectures: A Power/Performance/Thermal View

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Main Goals

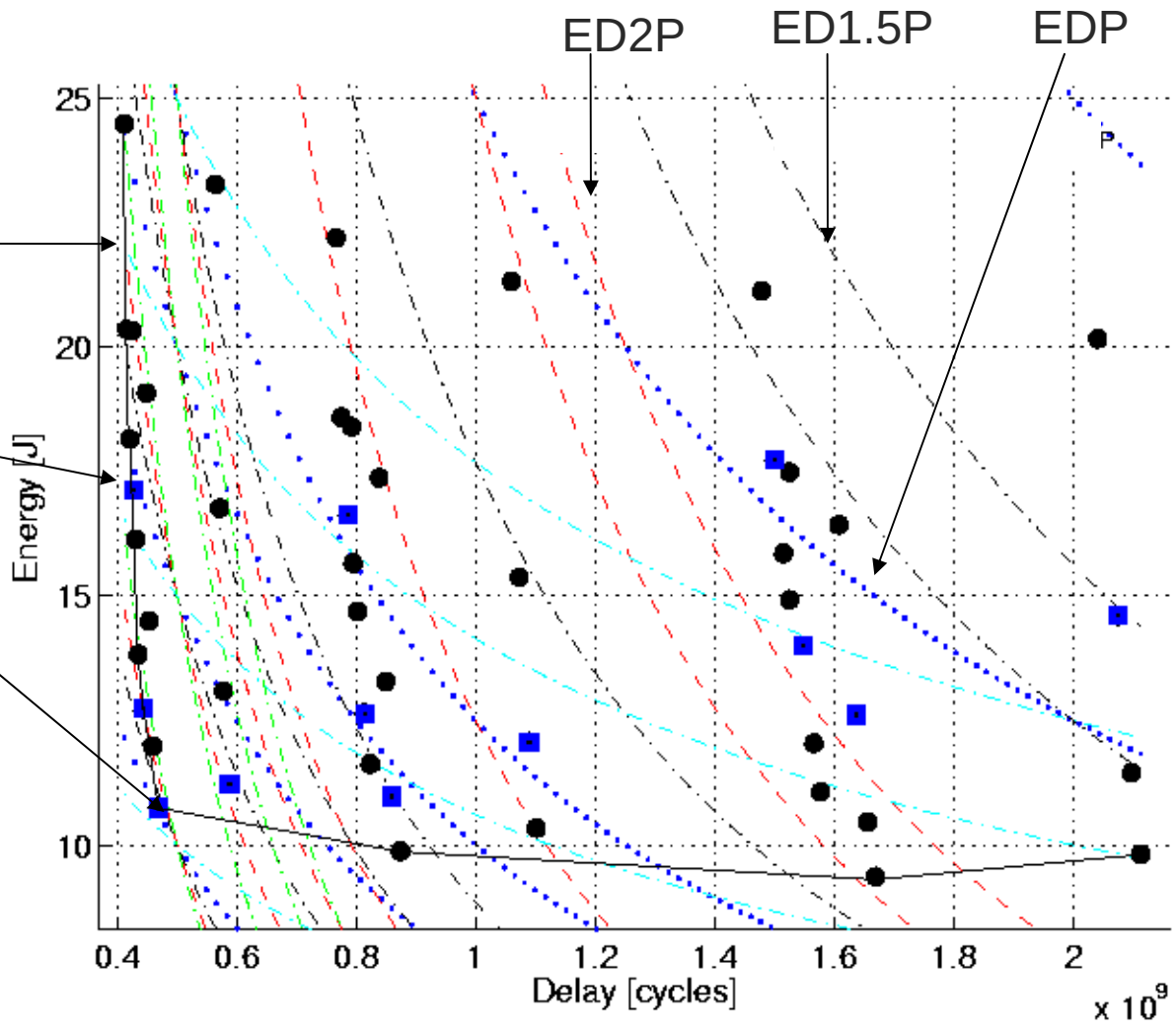
- Exploration of private-L2 shared memory Chip Multiprocessors
- Understanding interactions among
  - Power consumption
  - Temperature
  - Chip floorplan

2-8 cores, 2-8 wide issue, 256KB-2M L2 caches

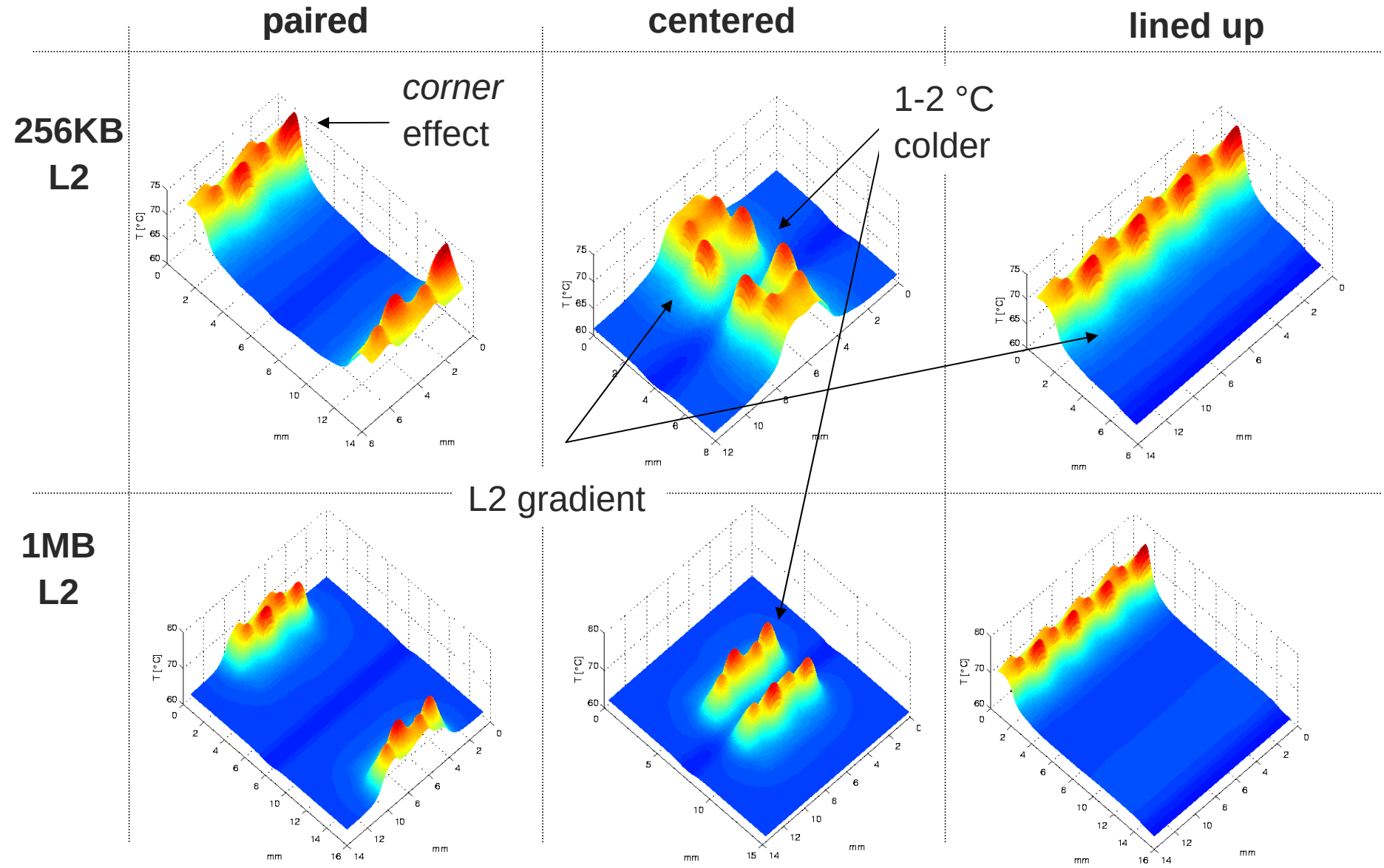
(Benchmarks: Splash-2, AlpBench)

Energy-Delay Trade-offs

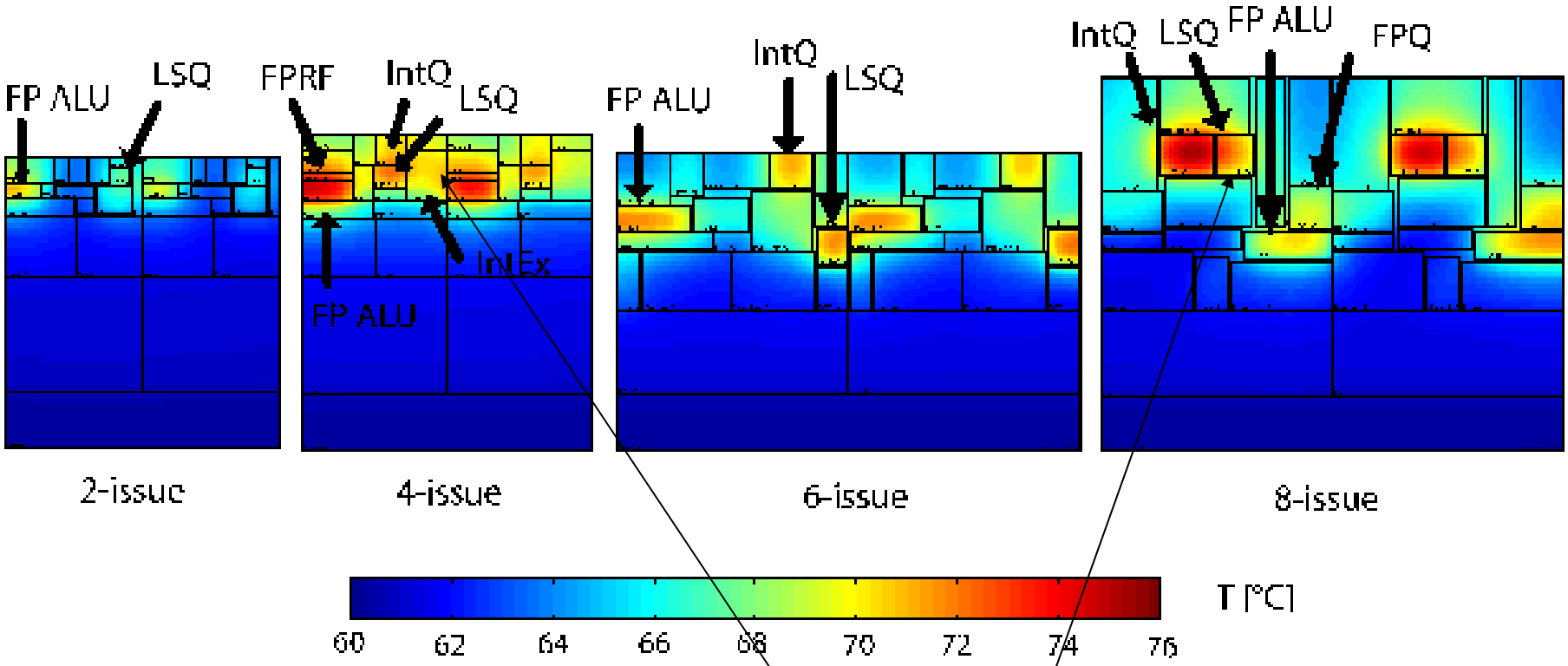
- Energy-efficient family
- Equivalent total L2 points
- Optimum is 8-core, 4-issue, 256KB-L2
- For ED2P and EDP



Floorplans Evaluation



Processor Complexity



- 2-core, 256KB-L2 and variable issue
- Hotspots:
  - FP ALU
  - LSQ e Int Queue for wide issue
- Inter-proc thermal coupling
- Intra-porc thermal coupling