Power/Performance/Thermal trade-offs in microarchitecture

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Main Goals

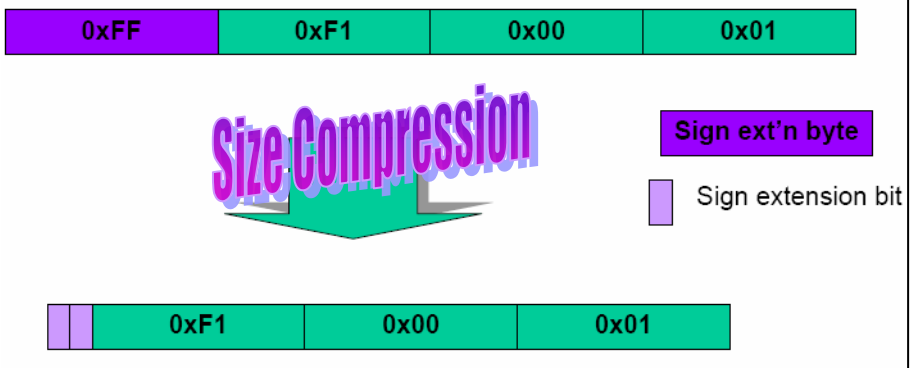
- Exploration of the power/thermal behaviour of architectures with value compression
- Compress values in all microarchitectural blocks
  - Size compression
  - Significance compression
  - Zero compression

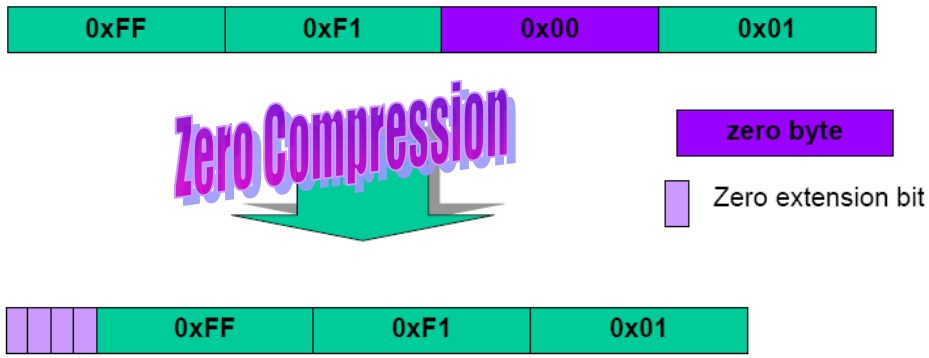
Single core, 4 wide issue, 64KB L1 cache, 2MB L2 cache

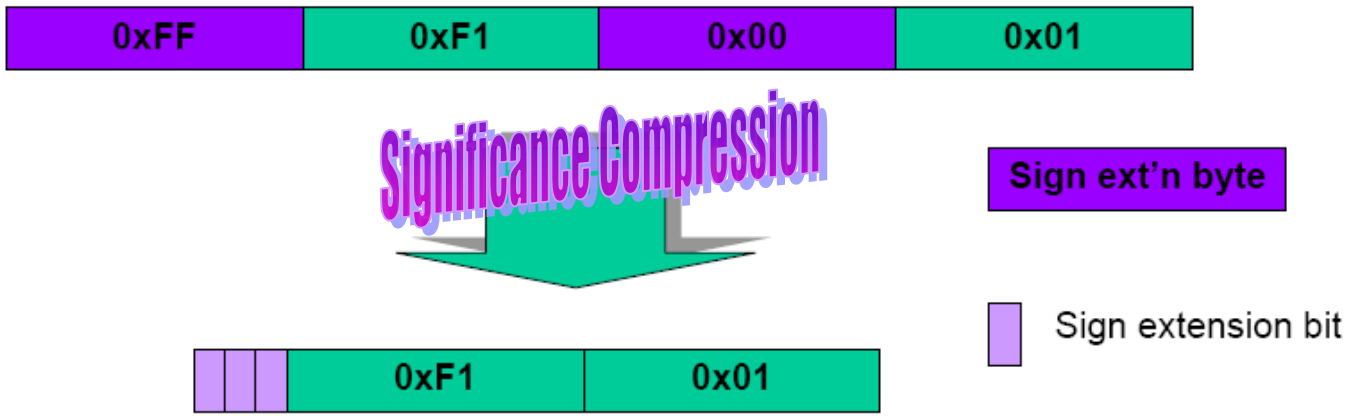
(Benchmark: Crafty -SpecInt2K-)

Value compression styles

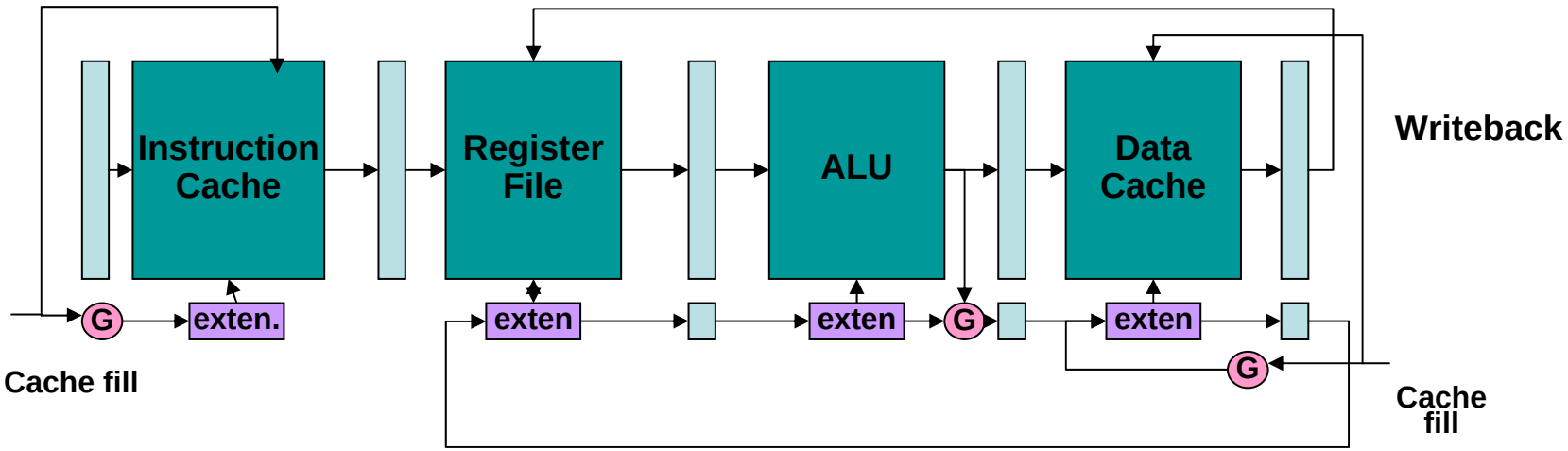
32-bit Value







Hw Value Compression

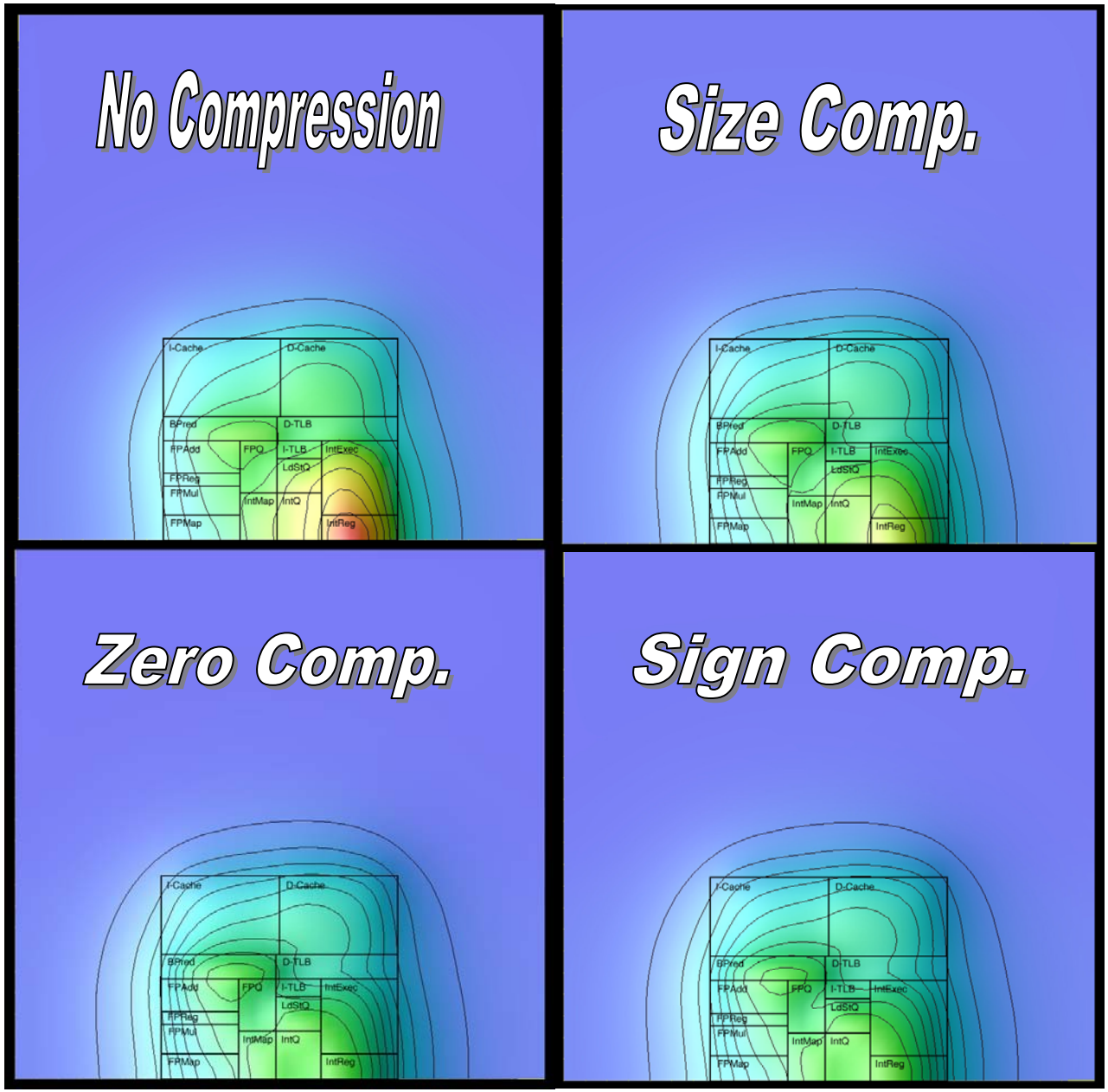


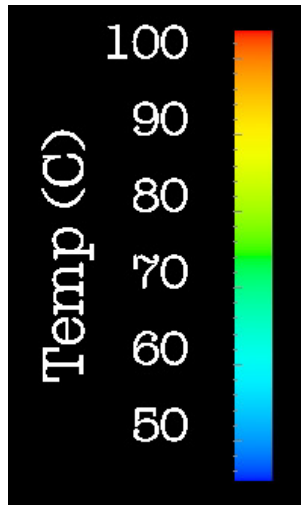
32-bit embedded processor pipeline with value compression

- Dynamically compress values flowing through the pipeline, with or without compiler help.
- Good for embedded and high performance processors!!

"Very Low Power Pipelines using Significance Compression", MICRO-33
"Software-Controlled Operand-Gating", CGO 2004
"Value Compression for Efficient Computation", EuroPar 2005

Thermal behaviour





Configurations used:

- Size 8-16-32-64
- Zero 8-16-24-32-40-48-56-64
- Sign 8-16-24-32-40-48-56-64