PREFACE

The synthesis of asynchronous circuits is one of the most complex —but at the same time challenging— problems investigated by the CAD community. Asynchronous circuits promise a number of important advantages over its synchronous counterparts for the design of large digital circuits. Its modularity, low power consumption, average computation time, and elimination of the clock distribution problem have encouraged an extensive analysis by multiple research groups. However, the synthesis of asynchronous circuits is inherently complex from two different aspects. Firstly, the required cumbersome theoretical analysis introduces restrictive correctness conditions that complicate the synthesis and minimization processes. Secondly, due to the inherent concurrency of the asynchronous circuits, even for small systems, they may contain several thousands or millions of states. This vast space of states requires an extremely costly computation process that most times cannot be successfully completed even in the more powerful available computers. This thesis tackles both aspects of the synthesis process from a new perspective overcoming both the complex analysis and computation complexity bottlenecks.

We start by introducing the synthesis problem from a formal modeling of the asynchronous circuits based on Petri nets. The target behavioral circuit specifications to be synthesized are described by means of a class of interpreted *free-choice* Petri nets named Signal Transition Graphs. Based on the mathematical formalization provided by the Signal Transition Graph model, the multiple steps that should be followed in the synthesis process are described, namely: the correctness of the specification, its binary coding properties, the implementability conditions, and finally the logic synthesis and minimization. Each one of these steps is efficiently implemented applying a set of structural methodologies that allow the efficient analysis of the Signal Transition Graph formalism without considering its associated underlying states.

The overall process has been integrated in a structural synthesis environment obtaining impressive results. Asynchronous circuits can be generated from STG specifications that exceed in several orders of magnitude the largest STG ever synthesized. However, not only the synthesized specifications are larger. Indeed, the computation times are also dramatically reduced, in some cases from days to a few seconds, and the area results are even optimized with gains with respect the current state-of-the-art techniques of about 30%.