Reza Yazdani Aminabadi

Personal Information

Date of Birth:	**15 March, 1989**
Marital status:	**Single**
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Education

- **[2015 – Now] Universitat Politecnica de Catalunya (UPC)**
  - **PhD researcher in Computer Architecture at ARCO group (http://arco.e.ac.upc.edu/wiki/)**
  - **Advisors: Jose-Maria Arnau, Antonio Gonzalez**
  - **Thesis: Ultra Low-Power, High-Performance Accelerators for Speech Recognition**
- **[2011 – 2014] University of Tehran, Tehran, Iran (ut.ac.ir)**
  - **Master of Computer Engineering in Computer Architecture**
  - **Advisor: Dr. Saeed Safari**
  - **Thesis : Increasing fault-tolerant capability of a reconfigurable NoC using reconfiguration both in its routing algorithm and architecture**
  - **Ranked among the best Master students of Computer Engineering-Computer Architecture, 2011 beginners**
  - **Master GPA = 3.84/4 (17.62/20)**
  - **Top Student in most of the Master courses**
  - **My Master courses are as follows:**
    - ✓ **Digital System Design Automation (RTL and ESL),** Instructor: Dr. Z. Navabi
    - ✓ **Advanced VLSI Design,** Instructor: Dr. Sied Mehdi Fakhraie
    - ✓ **Low Power Design,** Instructor: Dr. Ali Afzali-Kusha
    - ✓ **Advanced Computer Architecture,** Instructor: Dr. Omid Fatemi
    - ✓ **Fault tolerant Systems,** Instructor: Dr. Saeed Safari
    - ✓ **Interconnection Networks (NoC),** Instructor: Dr. Mehdi Modaressi
    - ✓ **Computer Arithmetic Algorithms,** Instructor: Dr. Saeed Safari
    - ✓ **Embedded System Processing Elements,** Instructor: Dr. Mostafa E Salehi
- **[2007 – 2011] Sheikh-Bahaee University, Isfahan, Iran (shbu.ac.ir)**
  - **Bachelor of Computer Engineering in Hardware Engineering**
  - **Thesis : Implementation of PID controller on a line-follower robot**
  - **Advisor: Dr. Kamal Jamshidi**
  - **Ranked 1st among all Bachelor students of Computer Hardware Engineering, 2007 beginners**

- **Undergraduate GPA = 3.86/4 (17.58/20)**
- **Top Student in Introduction to Algorithms with grade 20**
- **Top Student in Theory of Languages and Automata with grade 20**
- **Top Student in Advanced Programming with grade 19.5**
- **Top Student in Advanced Microprocessor with grade 19**
- **Top Student in Logic Circuits with grade 18.3**
- **Top Student in Electronics with grade 20**
- **Top Student in Digital Electronics with grade 20**
- **Top Student in VLSI Design with grade 18.14**

- **[2003 – 2007] Shahid-Beheshti High School , Esfahan , Iran**
  - **Diploma in Math and Physics.**

Teaching

- **TA of Fault-tolerant System Design, Administrator: Dr. Saeed Safari, [Fall 2014], [University of Tehran]**
- **TA of Computer Architecture Lab, Administrator: Dr. Saeed Safari, [Fall 2014], [University of Tehran]**
- **TA of Computer Architecture, Administrator: Dr. Saeed Safari, [Spring 2014 and Fall 2013], [University of Tehran]**
- **TA of Advanced Computer Architecture, Administrator: Dr. Omid Fatemi, [Fall 2012], [University of Tehran]**
- **TA of Theory of Languages and Automata, Administrator: Kazim Fouladi, [Fall 2012] ,[University of Tehran]**
- **TA of Electrical Circuits 1, Administrator: Mohammadreza Rezaeian, [Spring 2009], [Sheikh-Bahaee University]**

Publications

1. Reza Yazdani, Albert Segura, Jose-Maria Arnau, Antonio Gonzalez, "***An ultra Low-Power Hardware Accelerator for Automatic Speech Recognition***", in the 49th Annual IEEE/ACM International Symposium on Microarchitecture, **MICRO-49**, 2016
2. Reza Yazdani, Hamed Sheidaeian, and Mostafa E. Salehi, "***A Fast Design Space Exploration for VLIW Architectures***", 22nd Iranian Conference on Electrical Engineering (**ICEE**), 2014.
3. S.H. Seyyedaghaei Rezaei, M. Modarressi, R.Yazdani, M.Daneshtalab, "***Fault-Tolerant 3-D Network-on-Chip Design using Dynamic Link Sharing***", in the Conference on Design, Automation and Test in Europe (**DATE'16**),Germany, 2016.

Research Interests

- **Cognitive Computing (Speech Recognition)**
- **Low-power architectures**
- **High-performance architectures**
- **Reconfigurable architectures and application-aware design**
- **VLSI Design**
- **Embedded System design and implementation**
- **Network-on-chip (architecture, micro-architecture, routing algorithm)**
- **Fault Tolerant architectures**

Skills

- **Programming Languages : C, C++, C#**
- **Digital System Design using VHDL, Verilog or SystemC**
- **Assembly Programming for X-86-family and ARM processors**
- **Web Programming : HTML, ASP.Net**
- **Scripting: Python, TCL and BASH**

Tools and simulators

- **ASIC Synthesis Tools: Synopsys Design Compiler, Cadence SoC Encounter**
- **Transistor level Design: Hspice, LEdit, SEdit**
- **FPGA Synthesis and Simulation: Altera Quartus , ModelSim**
- **Embedded System Design: IAR Embedded WorkBench (ARM), ISE (FPGA), CodeVision (AVR), Proteus and Protel (PCB Design)**
- **Programming: Microsoft Visual Studio (Windows), Eclipse (Linux)**
- **Architecture Simulator and Framework : BookSim,Vex, SimpleScalar**
- **Operating Systems : Microsoft Windows Family , Linux (Ubuntu, Cent OS, Fedora, Suse)**

Language Expertise

- **Persian : Native**
- **English :**
  - **TOEFL IBT :**
    - ✓ **Took a test on January 25th, 2015 : Score: 98 (24, 26, 23, 25)**
  - **Certificate of Studying 12 Terms in Iran Language Institute:**
    - ✓ **Pre-Intermediate to Advanced level**

Academic Projects

- **Design a Viterbi search accelerator for Automatic Speech Recognition systems, 2015-2016**
  - ✓ Develop a simulator for the accelerator
  - ✓ Model the design at hardware using Verilog
  - ✓ Synthesize the accelerator using Synopsis Design Compiler and Cacti
- **Advanced VLSI Design, Fall 2012**
  - ✓ Synthesis and time/area optimization of a simplified MIPS processor using Synopsys Design Compiler tool
  - ✓ Placement and Routing a synthesized MIPS Processor using Cadence SoC Encounter tool
  - ✓ Designing schematic of a 3-bit MAC Unit using S-EDIT and conversion of it to layout using auto place and route tool of L-EDIT
  - ✓ Design of a Standard Cell Layout Full-Adder with LEdit and Post Layout Simulation using HSPICE
  - ✓ Study the Impacts of process, voltage and temperature variations on noise margins, propagation delays and power consumption of Inverter Ring Oscillator
- **Low Power Design, Spring 2012**

- ✓ Implementation and reproducing the result of “Design and Analysis of Two Low Power Cell Architectures”, IEEE Transactions on VLSI Systems, 2009.

- **Fault Tolerant Systems and Design, Fall 2011**
  - ✓ Implementation and reproducing the result of "A low-overhead and reliable switch architecture for Networks-on-Chip", Integration, the VLSI Journal, 2010.
  - ✓ RTL Fault Simulation and Injection on Sayeh processor by writing PLI code
  - ✓ Calculate the architectural vulnerability factor (AVF) with Sim-SODA
  - ✓ Evaluating the effect of transistor size on the SRAM soft errors with Hspice
- **Digital System Design Automation, Fall 2011**
  - ✓ Core Modeling and Design: Managing a Bus system using an arbiter
  - ✓ Hierarchical Design: Implementing different designs of a M×N crossbar network
  - ✓ Abstract Handshaking: Design of a serial-to-parallel converter
  - ✓ Design of Sayeh processor with SystemC and implement its handshaking with a memory unit using TLM

Presentations

- **The Next-Generation 64b SPARC Core in a T4 SoC Processor**
  Instructor: Dr. Sied Mehdi Fakhraie [Fall 2012] [University of Tehran]
- **A Survey on Design Space Exploration Methods**
  Instructor: Dr. Mostafa E Salehi [Spring 2012] [University of Tehran]
- **A reliable low-overhead switch architecture**
  Instructor: Dr. Saeid Safari [Fall 2011] [University of Tehran]
- **Implementation of modified tomasulo’s algorithm in MIPS architecture**
  Instructor: Dr. Omid Fatemi [Fall 2011] [University of Tehran]

Industrial Projects

- **Design and implementation of ECG signal simulator for calibration purpose in Khorshid Hospital of Isfahan, Iran.**
- **Design and implementation of PBX logger for telephone santrals in Panasonic Agent of Isfahan, Iran.**
- **Design and implementation of an accelerometer for laboratory purpose in Sheikh-Bahaee University of Isfahan, Iran.**
- **Design and implementation of an IC-Tester for laboratory purpose in Sheikh-Bahaee University of Isfahan, Iran.**
- **Implementing of a SD-Logger for logging medical data for long durations in Saadat Company of Tehran, Iran.**
- **Developing an In-Application-Programmer for STM32F103 ARM Micro-Controller using its boot-loader section in Saadat Company of Tehran, Iran.**
- **Programming a driver for PAN1740 BLE in one of Saadat company’s devices namely ECG-patch using Dialog-Semiconductor SDK3.0.4**