

Ramon Canal Corretger

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Departament d'Arquitectura de Computadors - Universitat Politècnica de Catalunya (UPC)

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Studies:

June 2004: **PhD. at the Departament d'Arquitectura de Computadors** of the UPC.

Thesis title: Power- and Performance- Aware Architectures *Qualification:* Excellent cum laude

Advisors: Antonio González (UPC) and James E. Smith (Univ. of Wisconsin-Madison).

1993-1998: **BSc. and Msc in Computer Science Engineering**, at UPC. Final year done at the **U. of Bath**, UK.

Honors and Awards:

2010: Recognition for Excellence in Education (2003-2007, evaluation every 5 years). Mèrits de docència d'especial qualitat (quinquenni 2003-2007). UPC and AQU Catalunya.

2010: HiPEAC Paper Award for the publication of “*An hybrid eDRAM/SRAM macrocell to implement first-level data caches*” in MICRO-42.

2008: First prize in the 6th Duran Farell Award in Excellence in Innovation and Technology (group member)

2008: IEEE Certificate of Appreciation in recognition of the inclusion of our paper in the compendium of the 10 most industry relevant and significant papers of 2007 in Computer Architecture.

2006: Fulbright Award. Fulbright Fellow and Visiting Scholar at Harvard University.

2001: First prize “Rosina Ribalta” of the Epson-Iberica Foundation to the best thesis project in Spain and Portugal.

2000: IBM Faculty Award for the work on value compression.

2000: Best student paper award at the “IEEE Sixth International Symposium on High Performance Computer Architecture” (HPCA-6).

Participation in projects:

Public administration:

European Level

- Key Personnel, Terascale Reliable Adaptive Memory Systems (TRAMS), European Union FP7, Oct. 2009–Sept. 2012
- Coordinator. “HW/SW Parallelism Exploitation in Chip Multiprocessor Architectures”, Spanish Ministry of Science and Technology – Italian Ministry of Science and Technology, sept. 2005–dec. 2007.
- Team leader. “Intelligent checkpointing for Kilo-Instruction Processors”, HiPEAC (NoE – European Union) reference HiPEAC-Cluster-19, sept. 2004–sept.2005.
- Research staff. Memory Hierarchy Analysis and Optimization Tools for the End-User (MHAOTEU), European Union, sept 1998–dec. 1999.

National Level

- PI. “A scalable and power-efficient memory hierarchy for CMPs”, Spanish Ministry of Science and Technology. 2008-2011
- PI. “On-die DRAM-based architectures”. Spanish Ministry of Education. 2009
- PI. “Reliability in the Face of Variability under Nanoscale Technology Scaling”. Spanish Ministry of Education. 2008
- Team Leader. “Microarquitectura i Compiladors”, Generalitat de Catalunya, 2009SGR1250. 2009–2013.
- Team Leader. “Arquitecturas y Compiladores 2”, Spanish Ministry of Science and Technology, 2008- 2010.

- Team Leader. “Microarquitectura i Compiladors”, Generalitat de Catalunya, 2005SGR00950. 2005 –2008.
- Research Staff. “Computación de Altas Prestaciones IV: Arquitecturas, Compiladores, Sistemas Operativos, Herramientas y Aplicaciones”, Spanish Ministry of Science and Technology, 2005-2007.
- Research staff. “Computación de Altas Prestaciones III: Arquitecturas, Compiladores, Sistemas Operativos, Herramientas y Algoritmos”, Spanish Ministry of Science and Technology, 2001-2004.
- Research staff. “Computación de Altas Prestaciones II: Arquitecturas, Compiladores, Sistemas Operativos y Aplicaciones”, Spanish Ministry of Science and Technology, 1998-2001.

Private funding/Industry:

- PI. “New Methods in Computer Architecture”, URL, 2003-2006.
- Research staff. “The subscalar microarchitecture”, IBM, Jan. 2000- Dec. 2000.

Publications: (H-index = 12, G-index = 25, Total refs: >600)

- *"Impact of Positive Bias Temperature Instability (PBTI) on 3T1D-DRAM Cells "*, N. Aymerich, S. Ganapathy, A. Rubio, R. Canal, A. González; IEEE/ACM Great Lakes Symposium on VLSI, Lausanne (Switzerland), May 2011
- *"An application-aware adaptive cache organization for tiled micro architectures "*, E. Herrero, J. González, R. Canal; Intel 2010 European Research and Innovation Conference, Braunschweig (Germany), September 2010
- *"Cache Design Under Spatio-Temporal Variability"*, S. Ganapathy, R. Canal, A. González, A. Rubio; Intel 2010 European Research and Innovation Conference, Braunschweig (Germany), September 2010
- *"Power-Efficient Spilling Techniques for Chip Multiprocessors"*, E. Herrero, J. González, R. Canal, International Conference on Parallel and Distributed Computing, (EURO-PAR'10), Ischia (Italy), August 2010
- *"MODEST : A Model for Energy Estimation under Spatio-Temporal Variability"*, S. Ganapathy, R. Canal, A. González, A. Rubio; 15th ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED 2010) , August 2010 (Austin, Texas)
- *"Elastic Cooperative Caching: An Autonomous Dynamically Adaptive Memory Hierarchy for Chip Multiprocessors"*, Enric Herrero, José González, Ramon Canal, IEEE/ACM 37th International Conference on Computer Architecture (ISCA'10), Saint-Malo (France), June 2010
- *"Circuit Propagation Delay Estimation Through Multivariate Regression-Based Modeling Under Spatio-Temporal Variability"*, S. Ganapathy, R. Canal, A. Rubio, A. González, IEEE Design, Automation and Test in Europe Conference (DATE'10), March 2010
- *"An hybrid eDRAM/SRAM macrocell to implement first-level data caches"*, A. Valero, J. Sahuquillo, S. Petit, V. Lorente, R. Canal, P. Lopez, J. Duato, IEEE/ACM International Symposium on Microarchitecture (MICRO-42), December 2009
- *"Using Coherence Information and Decay Techniques to Optimize L2 Cache Leakage in CMPs"*, M. Monchiero, R. Canal, A. González, IEEE 38th International Conference on Parallel Processing (ICPP-2009), Vienna (Austria), Sept. 2009.
- *"Distributed Cooperative Caching"*, E. Herrero, J. González, R. Canal, IEEE/ACM 17th International Conference on Parallel Architectures and Compilation Techniques (PACT), Toronto (CA), Oct. 2008.
- *"A Scalable and Power-Efficient Memory Hierarchy for Multicore Architectures"*, E. Herrero, J. González, R. Canal, Intel 2008 European Research and Innovation Conference, Leixlip (Ireland), September 2008. –Poster–
- *"DRAM-based On-Chip Cache Architectures to Combat Process Variations"*, X. Liang, R. Canal, G.Y. Wei, D. Brooks, Intel 2008 European Research and Innovation Conference, Leixlip (Ireland), September 2008. –Poster–
- *"Power/Performance/Thermal Design Space Exploration for Multicore Architectures"*, M. Monchiero, R. Canal, A. González, IEEE Transactions on Parallel and Distributed Systems, v. 19 n. 5 pp.666-681, May 2008.
- *"Replacing 6T SRAMs with 3T1D DRAMs in the L1 Data Cache to Combat Process Variability"*, X. Liang, R. Canal, G.Y. Wei, D. Brooks, IEEE Micro Micro's Top Picks from Computer Architecture Conferences, Jan 2008

- “*Process Variation Tolerant 3T1D-Based Cache Architectures*”, X. Liang, R. Canal, G.Y. Wei, D. Brooks, The 40th International Symposium on Microarchitecture (MICRO-40), December 2007 (Chicago, Illinois)
- “*Process Variation Tolerant Register Files Based on Dynamic Memories*”, X. Liang, R. Canal, G.Y. Wei, D. Brooks, ASGI'07, Workshop on Architectural Support for Gigascale Integration (In conjunction with ISCA 2007), June 2007 (San Diego, California)
- “*Design Space Exploration for Multicore Architectures: A Power/Performance/Thermal View*”, M. Monchiero, R. Canal, A. González, ACM International Conference on Supercomputing (ICS-06), Cairns (Australia), June 2006.
- “*Design Space Exploration for Multicore Architectures: A Power/Performance/Thermal View*”, M. Monchiero, R. Canal, A. González, Intel 2006 Academic Forum, Dublin (Ireland), June 2006. –Poster–
- “*Power/Performance/Thermal trade-offs in microarchitecture*”, D.Oro, R. Canal, A. González, James E. Smith, Intel 2006 Academic Forum, Dublin (Ireland), June 2006. –Poster–
- “*Value Compression for Efficient Computation*”, R. Canal, A. González and James E. Smith, Lecture Notes in Computer Science, v. 3648, pp. 519-529, Springer-Verlag, 2005.
- “*Software-Controlled Operand-Gating*”, R. Canal, A. González and James E. Smith, 2004 International Symposium on Code Generation and Optimization, Palo Alto (CA), March 2004.
- “*Power and Complexity Aware Microarchitectures*”, J. Abella, R. Canal, A. González, Intel 2004 Academic Forum, Barcelona (Spain), 2004. –Poster–
- “*Power- and Complexity-Aware Issue Queue Designs*”, J. Abella, R. Canal and A. González, IEEE Micro Special Issue on Power- and Complexity-Aware Design, vol. 29 n. 5, pp. 50-59, Sept. 2003.
- “*Reducing the Complexity of the Issue Logic*”, R. Canal, A. González, ACM International Conference on Supercomputing (ICS-01), Sorrento (Italy), June 2001.
- “*Dynamic Code Partitioning for Clustered Architectures*”, R. Canal, J.M. Parcerisa and A. González, International Journal of Parallel Processing, vol 29 n. 1, 2001.
- “*Low Power Pipelines using Significance Compression*”, R. Canal, A. González and James E. Smith, International Symposium on Microarchitecture (MICRO-33), Monterey (CA) Dec. 2000.
- “*A Low-Complexity Issue Logic*”, R. Canal, A. González. ACM International Conference on Supercomputing (ICS-00), Santa Fe (NM), May 2000.
- “*Dynamic Cluster Assignment Mechanisms*”, R. Canal, J.M. Parcerisa and A. González, Int. Symposium on High Performance Computer Architecture (HPCA-6), Toulouse, Jan. 2000. *Best Student Paper Award*.
- “*A Cost-Effective Clustered Architecture*”, R. Canal, J.M. Parcerisa and A. González, IEEE/ACM 8th International Conference on Parallel Architectures and Compilation Techniques (PACT), Newport Beach, Oct. 1999.

Invited talks:

- “*Memory Organization in the Multi/Many-Core Era*”, Intel Microprocessor Technology Lab, Hillsboro, Oregon 15/02/2011
- “*Run-time PVT variations monitoring and adaptation*”, Intel Circuit Research Lab, Hillsboro, Oregon 15/02/2011
- “*Reliability: next big challenge*”, U. Politècnica de València, València, 17/11/2010
- “*Future trends and challenges in the microprocessor world*”, U. del Turabo, Caguas, Puerto Rico, 2/3/2007
- “*Future trends and challenges in the microprocessor world*”, U. Metropolitana, San Juan, Puerto Rico, 2/3/2007
- “*Computer architecture research by the Mediterranean*”, Department of Electrical and Computer Engineering, Harvard University, Cambridge (MA-USA), 25/10/2006

- “*How to keep cool and get the job done*”, NU Computer Architecture Research Group, Northeastern University, Boston (MA-USA), 29/6/2006
- “*Low Power Pipelines using Significance Compression*”, Microsystems Design Laboratory, Penn State University, Pittsburgh (PA-USA), 01/12/2000

Professional Experience:

Current:

- * Deputy Head of the Department of Computer Architecture of the Universitat Politècnica de Catalunya, Spain (May 2008- now).
- * Coordinator of the Computer Engineering Speciality, Computer Science School (UPC), June 2010-now.
- * Associate professor at the Department of Computer Architecture at the Computer Science Faculty of the Universitat Politècnica de Catalunya, Spain (April 2008- now). Teaching Microprocessor Design, Computer Design and Technology (all Master/PhD. courses).

Previous:

- * Assistant professor at the Department of Computer Architecture at the Computer Science Faculty of the Universitat Politècnica de Catalunya, Spain (September 2003- April 2008). Teaching Microprocessor Design, Computer Design and Technology and Computer Architecture (all Master/PhD. courses).
- * Invited Lecturer at the School of Engineering of the Universitat Ramon Llull (URL), Spain (2003-2006).
- * Summer intern at the “Sparc Architecture Group” of Sun Microsystems in Sunnyvale (California, EEUU), July - October 2000.
- * Part-time assistant professor at the Telecommunications Faculty of the Universitat Politècnica de Catalunya (September 1999 - February 2000). Teaching Introduction to Computers.

Parallel research/academia activities:

- * Program committees served:
 - * 38th IEEE/ACM International Symp. on Computer Architecture (ISCA), San Jose (USA), June 2011.
 - * 2nd Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures, in conjunction with ARCS2011, February 2011.
 - * 17th IEEE International Conference on High Performance Computing, Goa (India), December 2010.
 - * 1st Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures, in conjunction with ARCS2010, February 2010.
 - * 25th IEEE International Parallel and Distributed Processing Symposium, Rome (Italy), May 2009.
 - * 15th IEEE International Conference on High Performance Computing, Bangalore (India), December 2008.
 - * 26th IEEE International Conference on Computer Design, Squaw Creek, Lake Tahoe (California, EE.UU.), October 2008.
 - * 13th IEEE International Conference on Parallel and Distributed Systems, Hsinchu (Taiwan), December 2007.
 - * 2007 ACM International Conference on Computing Frontiers, Ischia (Italy), May 2007.
 - * IEEE 24th International Conference on Computer Design, San Jose (California-USA), October 2006.
 - * 12th International Conference on Parallel and Distributed Systems, Minneapolis (Michigan-USA), July 2006.
 - * Reviewer for several (IEEE and ACM) conferences and journals such as: MICRO, HPCA, ISCA, PACT, ICS, EUROPAR, CGO, IPDPS, IPADS, ICCD, IEEE Micro, IEEE Micro Top Picks, IEEE Transactions on Computers, IEEE Transaction on VLSI Systems, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Evolutionary Computing, IET Circuits, Devices & Systems, ACM Transactions on Architecture and Code Optimization, Journal of Systems Architecture, ACM Computer Architecture Letters.
- * Conference organization committees:
 - * Organization committee of the 17th IEEE International On-Line Testing Symposium, Tossa de Mar, (Catalonia), July 2011.
 - * Webmaster of the 33rd ACM/IEEE Annual International Symposium on Computer Architecture, Boston (Massachusetts-USA), June 2006.

- * Webmaster of the 37th ACM/IEEE International Symposium on Microarchitecture (Micro-38), Portland (Oregon-USA), December 2004.
- * Other committees served:
 - * Member of the selection committee of project proposals for the Nederlandse Organisatie voor Wetenschappelijk Onderzoek - Netherlands Organisation for Scientific Research (NWO). July 2009.
 - * Fulbright Selection Committee, Generalitat de Catalunya, 2008 and 2009.

Other merits:

Acreditaciones/Habilitaciones (Accreditations for the different professor positions):

Consejo de Coordinación Universitaria

- Habilitación Nacional para el cuerpo de profesores titulares de universidad (25/05/2007)

Agencia Nacional de Evaluación de la Calidad y Acreditación (ANECA)

- Acreditación de profesor contratado doctor (3/07/2007)
- Acreditación de profesor de universidad privada (3/07/2007)
- Acreditación de profesor ayudante doctor (18/05/2005)
- Acreditación de profesor colaborador (30/05/2003)

Agència per a la Qualitat del Sistema Universitari de Catalunya (AQU)

- Acreditación de profesor de universidad privada (20/04/2006)
- Acreditación de profesor lector (18/04/2005)
- Acreditación de profesor colaborador (28/07/2003)

Evaluation of the succesful completion of research periods (every 6 years):

Generalitat de Catalunya and Spanish Ministry of Science and Innovation

1 Sexenio de investigación reconocido (2000-2005)

Consultancy:

- Editorial Pearson Educación/Prentice Hall (2006) evaluation of the book to determine the impact in graduate level courses at Spanish universities. “Microprocesadores Intel: arquitectura, programación e interfaz.”, séptima edición, Barry B. Brey, Pearson Educación/Prentice Hall, ISBN: 970-26-084-X
- Editorial Reverté (2005) evaluation of the book to determine the impact of a translation. “Computer Organization and Design. The Hardware/Software interface”, J.L. Hennessy y D.A. Patterson, Morgan-Kaufman, 2004, ISBN: 978-1-55860-604-3